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(71)Applicant : ANRITSU CORP
(72)Inventor : SAITO SUMIO

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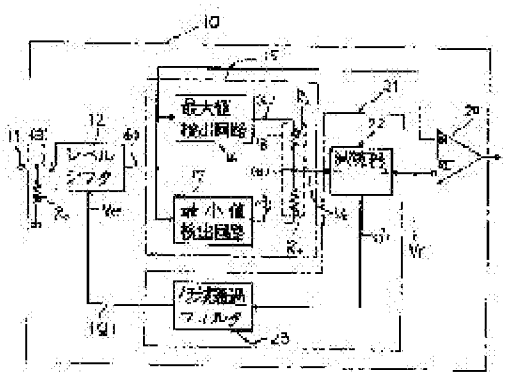
(54) WAVEFORM SHAPING CIRCUIT AND DIGITAL SIGNAL ANALYZER

(57)Abstract:

PURPOSE: To apply stable waveform shaping to an inputted digital signal without being affected by its amplitude change or an offset.

CONSTITUTION: An inputted digital signal is inputted to an intermediate voltage detection circuit 15 via a level shifter 12. The intermediate voltage detection circuit 15 detects an intermediate voltage V0 between a high level and a low level of the inputted digital signal and outputs the voltage to a subtractor 22 of a control circuit 21. The control circuit 21 outputs a difference signal between the intermediate voltage V0 and the reference voltage Vr to the level shifter 12 via a low pass filter 25 to control the shift of the level shifter 12 in a direction that the intermediate voltage V0 approaches the reference voltage Vr. The digital signal subjected to level shift by the level shifter 12 is inputted to a comparator 20 using the reference voltage Vr as a threshold voltage, in which the signal is subjected to waveform shaping.



CLAIMS

[Claim(s)]
[Claim 1]A level shifter (12) which carries out variable control of the direct current offset voltage of an inputted digital signal, A comparator (20) which shapes in waveform and outputs a digital signal outputted from this level shifter as compared with predetermined reference voltage, An intermediate voltage detection means (15) to detect and output middle voltage of high-level voltage of a digital signal and low-level voltage which were outputted from said level shifter, A waveform shaping circuit provided with a control means (21) which outputs a control signal to which said direct current offset voltage is changed in response to middle voltage and said predetermined reference voltage which are outputted from this intermediate voltage detection means in order to make said middle voltage equal to said predetermined reference voltage to said level shifter.
[Claim 2]A waveform shaping circuit given [provided with holding mechanism (25) holding said control signal outputted from said control means, and the means for stopping (26) and (27) which stops an operation of said intermediate voltage detection means when said control signal is held by this holding mechanism] in the 1st paragraph.
[Claim 3]A level shifter (52) which carries out variable control of the direct current offset voltage of an inputted digital signal, A comparator (60) which shapes in waveform and outputs a digital signal outputted from this level shifter as compared with predetermined reference voltage, An intermediate voltage detector circuit (55) which detects and outputs middle voltage of high-level voltage of a digital signal and low-level voltage which were outputted from said level shifter, Middle voltage and said predetermined reference voltage which are outputted from this intermediate voltage detector circuit are received, The 1st control means (61) that outputs a control signal to which said direct current offset voltage is changed to said level shifter in order to make said middle voltage equal to said predetermined reference voltage, A variable delay device (71) which changes relatively a phase between an inputted clock signal and an output of said comparator, A discrimination circuit (72) which receives an output and said clock signal of said comparator into which a phase was relatively changed by this variable delay device, and judges numerals of an output signal of a standup of this clock signal, or said comparator at the time of falling, An error measuring instrument (75) which compares a decision signal from this discrimination circuit with a reference signal equivalent to said inputted digital signal, and outputs an error signal, A digital-signal-analysis device provided with the 2nd control means (80) that decreases said error signal which detects an almost middle delaying amount of a delaying amount from which an error signal becomes ******** with the maximum in response to an

output of this error measuring instrument, and sends out this middle delaying amount to said variable delay device, and said error measuring instrument outputs.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application]This invention relates to the digital-signal-analysis device which analyzes the waveform shaping circuit which shapes in waveform and outputs the digital signal inputted, and the digital signal inputted like a logic analyzer or an error measuring device synchronizing with a clock signal.
[0002]
[Description of the Prior Art]Generally, after shaping in waveform the digital signal inputted from the outside by the waveform shaping circuit which comprises a comparator, it comprises digital-signal-analysis devices mentioned above, such as a logic analyzer and an error measuring device, so that the binary judging may be performed.
[0003]It is necessary to set it as the best operating point which corresponds to offset of the digital signal into which the operating point of a comparator is inputted, and is not influenced by a noise in this kind of waveform shaping circuit. In order to set up this operating point, either of the following three methods was carried out conventionally.
[0004](1) The technique of setting the threshold level (reference voltage) to a comparator as an optimum state manually, while monitoring the output wave of a comparator.
[0005](2) A technique make the digital signal inputted input into a comparator via a capacitor, and excluding the influence of offset.
[0006](3) A technique which carries out manual variable by a level shifter beforehand supposing the direct-current average level of the digital signal inputted, and is inputted into a comparator.
[0007]However, in (1) or (3) technique mentioned above, whenever operating point setting out by hand control is troublesome and the level of an input signal and offset change, the setting-operation must be performed.
[0008]In the technique of (2) mentioned above, the threshold which the offset voltage of the digital signal inputted into a comparator according to the mark rate (ratio of the total number of bits to generate and the number of marks contained in it) of the digital signal inputted changed and fixed cannot perform positive waveform shaping.
[0009]For this reason, the technique inputted into a comparator by making high-level voltage of the digital signal inputted and intermediate voltage of low-level voltage into a threshold is also considered.
[0010]However, in the case of the comparator of the large comparison low speed of a common mode input range, this technique is effective, but. Like the comparator for shaping the signal of ultrahigh frequency (several gigahertz) in waveform, when a common mode input range is very narrow, the comparator itself is saturated by change of the offset voltage of an input signal, and there is a problem that normal waveform-shaping operation cannot be performed.
[0011]On the other hand, the binary judging of the digital signal which shaped in waveform is performed, and the digital-signal-analysis device which analyzes the digital data is constituted as shown in drawing 17 from the former.
[0012]That is, waveform shaping of the data signal under test inputted into one input terminal 1 is carried out by the comparator 3 which makes a threshold reference voltage Vr from the

reference voltage generator 2. Since this reference voltage Vr is beforehand set as the best value by either of the techniques mentioned above, the fluctuation ingredient of the amplitude direction of the data signal under test shown in (a) of drawing 18, As shown in (b) of the figure, waveform shaping is carried out, and it is inputted into data input terminal D of the discrimination circuit 4 which comprised a D type flip-flop.

[0013]The clock signal inputted into the input terminal 5 of another side is inputted into clock terminal CP of the discrimination circuit 4 via the variable delay device 6.

[0014]This variable delay device 6 is beforehand adjusted so that a clock signal may rise to the timing whose binary level of the data signal inputted into the discrimination circuit 4 is most stable.

[0015]The output signal of the comparator 3 shown in (b) of drawing 18 as this adjustment, displaying the clock signal shown in (c) of the figure on a dual trace oscilloscope -- the standup timing of a clock signal -- the change state points I and II of a digital signal -- so that it may be located mostly at the halfway point (point that the phase margin is the largest), The method of adjusting the delaying amount of the variable delay device 6 with hand control was taken conventionally.

[0016]Thus, discernment of a binary is made to the standup timing of a clock signal of inputting the digital signal from the comparator 3 into the discrimination circuit 4, the decision output is inputted into the data analysis part 7 with a clock signal, and predetermined data analysis is conducted.

[0017]However, in such a conventional digital-signal-analysis device of composition, in addition to the hand regulation of the waveform shaping circuit mentioned above, hand regulation of the delaying amount also had to be performed, it was easy to produce the difference of these preset values according to the operator's individual difference, and there was a problem that a difference will appear also in an analysis result.

[0018]When adjusting by carrying out waveform observation with an oscilloscope, connection between apparatus is not only complicated, but by connection of an oscilloscope, the waveform of a signal may be confused and it may cause malfunction. As especially mentioned above, in connecting the cable for waveform observation to the signal of ultrahigh frequency (several gigahertz), adjustment with it becomes difficult. [this wave-like large disorder and] [exact]

[0019]For this reason, although the technique of providing the monitor terminal for waveform observation was also in the digital-signal-analysis device, there was no change in always having to prepare apparatus for waveform observation, such as an oscilloscope, and it was dramatically inconvenient.

[0020]An object of this invention is to provide the waveform shaping circuit and digital-signal-analysis device which solved the problem mentioned above.

[0021]

[Means for Solving the Problem]In order to solve said SUBJECT, a waveform shaping circuit of this invention, A level shifter (12) which carries out variable control of the direct current offset voltage of an inputted digital signal, A comparator (20) which shapes in waveform and outputs a digital signal outputted from this level shifter as compared with predetermined reference voltage, An intermediate voltage detection means (15) to detect and output middle voltage of high-level voltage of a digital signal and low-level voltage which were outputted from said level shifter, In response to middle voltage and said predetermined reference voltage which are outputted from this intermediate voltage detection means, in order to make said middle voltage equal to said predetermined reference voltage, it has a control means (21) which outputs a control signal to

which said direct current offset voltage is changed to said level shifter.
[0022]A level shifter (52) which carries out variable control of the direct current offset voltage of a digital signal into which a digital-signal-analysis device of this invention was inputted, A comparator (60) which shapes in waveform and outputs a digital signal outputted from this level shifter as compared with predetermined reference voltage, An intermediate voltage detector circuit (55) which detects and outputs middle voltage of high-level voltage of a digital signal and low-level voltage which were outputted from said level shifter, Middle voltage and said predetermined reference voltage which are outputted from this intermediate voltage detector circuit are received, The 1st control means (61) that outputs a control signal to which said direct current offset voltage is changed to said level shifter in order to make said middle voltage equal to said predetermined reference voltage, A variable delay device (71) which changes relatively a phase between an inputted clock signal and an output of said comparator, A discrimination circuit (72) which receives an output and said clock signal of said comparator into which a phase was relatively changed by this variable delay device, and judges numerals of an output signal of a standup of this clock signal, or said comparator at the time of falling, An error measuring instrument (75) which compares a decision signal from this discrimination circuit with a reference signal equivalent to said inputted digital signal, and outputs an error signal, It has the 2nd control means (80) that decreases said error signal which detects an almost middle delaying amount of a delaying amount from which an error signal becomes ******** with the maximum in response to an output of this error measuring instrument, and sends out this middle delaying amount to said variable delay device, and said error measuring instrument outputs.
[0023]
[Function]Since it is constituted in this way, in the waveform shaping circuit of this invention, the digital signal inputted is inputted into a comparator via a level shifter, and waveform shaping is carried out by predetermined reference voltage. The high-level voltage of the digital signal outputted from a level shifter and the middle voltage of low-level voltage are detected by an intermediate voltage detection means, and are outputted to a control means with reference voltage. A control means outputs a control signal for middle voltage to become equal to reference voltage to a level shifter, and changes the direct current offset voltage of the digital signal inputted.
[0024]In the digital-signal-analysis device of this invention, a phase in the meantime is changed by the variable delay device, and the clock signal inputted from the output signal and input terminal of the comparator by which waveform shaping was carried out in the waveform shaping circuit of the above-mentioned invention and the waveform shaping circuit of the identical configuration is inputted into a discrimination circuit. The decision signal from a discrimination circuit is compared with the reference signal which is equivalent to the inputted digital signal with an error measuring instrument. The error signal detected by the error measuring instrument is inputted into the 2nd control means. the delaying amount from which the delaying amount of a variable delay device is changed, and an error signal becomes ******** with the maximum while the 2nd control means receives the error signal from an error measuring instrument -- a middle delaying amount is detected mostly and it outputs to a variable delay device.
[0025]
[Example]Hereafter, the 1st example of this invention is described based on a drawing.
[0026]Drawing 1 is a circuit diagram showing the composition of the waveform shaping circuit 10 of the 1st example.
[0027]In drawing 1, the termination of the input digital signal inputted into the terminal 11 is

carried out by input-resistance R_0 (for example, 50ohms), and it is inputted into the level shifter 12.

[0028]The level shifter 12 changes the average direct-current (offset) voltage level of an input digital signal according to the size of the error signal (control signal) Ve from the control circuit 21 mentioned later. For this reason, the level shifter 12 is constituted as shown, for example in drawing 2.

[0029]That is, the average direct current voltage of an input digital signal is detected in the integration circuit by resistance R_1 and capacitor C_1, and is inputted into the adding machine 13. The adding machine 13 adds the error signal Ve to this average direct current voltage, and outputs that added voltage via resistance R_2. Between resistance R_2 and the terminal 11, capacitor C_2 which passes only the alternating current component of an input digital signal is provided. Therefore, from the node of capacitor C_2 and resistance R_2, the signal with which the level was shifted only for the error voltage Ve is outputted to the signal with which the output voltage from the adding machine 13 was applied to the alternating current component of an input digital signal, i.e., an input digital signal.

[0030]Resistance R_1 and R_2 have the high resistance about [which does not have influence in the transmission impedance of 50 ohms] number 10Komega.

[0031]The output of the level shifter 12 is inputted into the intermediate voltage detector circuit 15 and the comparator 20 mentioned later as shown in drawing 1.

[0032]The maximum detector circuit 16 where the intermediate voltage detector circuit 15 detects the maximum voltage of the output signal of the level shifter 12, It is constituted by the intermediate voltage output circuit 18 which outputs the middle voltage between the output voltage of the minimum value detecting circuit 17 which detects the minimum voltage of the output signal of the level shifter 12, and both the detector circuits 16 and 17 from the node of two resistance R_3 of the same resistance by which the series connection was carried out mutually, and R_4.

[0033]The comparator 20 outputs high level, when the level of the output signal of the level shifter 12 inputted into one input terminal IN is larger than the predetermined reference voltage (henceforth threshold voltage) Vr applied to the input terminal REF of another side, and when small, it outputs the digital signal of a low level. This comparator 20 comprises a semiconductor device for ultrahigh frequency (for example, gallium arsenide type FET), etc.

[0034]The middle voltage Vo outputted from the intermediate voltage detector circuit 15 and the threshold voltage Vr are inputted into the control circuit 21 which is a control means of this waveform shaping circuit 10. The control circuit 21 detects the difference of the middle voltage Vo and the threshold voltage Vr which are inputted with the subtractor 22, and outputs the difference voltage signal to the level shifter 12 via the low pass filter 23, The middle voltage Vo controls the shift amount of the level shifter 12 in the direction which is in agreement with the threshold voltage Vr.

[0035]Drawing 3 shows an example of the more concrete circuit of the intermediate voltage detector circuit 15 and the control circuit 21.

[0036]Namely, the diode 16a by which the anode side was connected to the output of the level shifter 12 in the maximum detector circuit 16, It has the Masakata-oriented peak detection circuit formed by the capacitor 16b connected with the cathode of the diode 16a between groundings, Between the node of this diode 16a and capacitor 16b, and predetermined negative supply-V_1, the constant current source 16c which sends very small forward bias current is connected to the diode 16a.

[0037]The diode 17a by which the cathode side was connected to the output of the level shifter 12 in the minimum value detecting circuit 17, It has a peak detection circuit of the negative direction formed by the capacitor 17b connected between the anode side of the diode 17a, and grounding, Between the node of the diode 17a and the capacitor 17b, and predetermined positive supply $+V_1$, the constant current source 17c which sends very small forward bias current is connected to the diode 17a.
[0038]Therefore, from the node of the diode 16a of the maximum detector circuit 16, and the capacitor 16b, The high-level voltage more than negative supply-V_1 voltage will be outputted among the digital signals outputted from the level shifter 12, and the low-level voltage below positive supply $+V_1$ voltage will be outputted from the node of the diode 17a of the minimum value detecting circuit 17, and the capacitor 17b.
[0039]The forward bias current from the constant current sources 16c and 17c over each diodes 16a and 17a hardly affects it to an input digital signal, but is set as the current value about [required to compensate the nonlinearity of detection operation of each diodes 16a and 17a moreover] 1microA.
[0040]The capacity value of the capacitors 16c and 17c is set as the value of about 1000 PF which can hold the peak value of the digital signal of 1 kHz or more of cycle periods in consideration of the forward bias current over each diodes 16a and 17a being a 1microA grade.
[0041]The subtractor 22 of the control circuit 21 is formed of the differential amplifier 22a and the feedback resister 22b, and the voltage according to the difference of the intermediate voltage Vo and the threshold voltage Vr is outputted from the differential amplifier 22a. The low pass filter 23 formed by the resistance 23a and the capacitor 23b outputs the error signal Ve excluding the noise component from the output of the differential amplifier 22a to the level shifter 12.
[0042]Therefore, since the output voltage of the differential amplifier 22a will rise if the middle voltage Vo falls to the threshold voltage Vr, the level of the digital signal which the error signal Ve goes up and is outputted from the level shifter 12 goes up to the whole. Conversely, since the output voltage of the differential amplifier 22a will decline if the middle voltage Vo rises to the threshold voltage Vr, the level of the digital signal which the error signal Ve falls and is outputted from a level shifter will fall to the whole.
[0043]Next, operation of the above-mentioned waveform shaping circuit 10 is explained.
[0044]Now, temporarily, the maximum of the digital signal inputted to the level shifter 12 by time t_0 and the mean value of the minimum presuppose that it is equal to the threshold voltage Vr of the comparator 20, as shown in (a) of drawing 4.
[0045]In this case, since the output of the subtractor 22 of the control circuit 21 serves as zero, the digital signal inputted into the level shifter 12 is inputted into the comparator 20 as it is, and waveform shaping is carried out on the threshold voltage Vr.
[0046]And in time t_1, as shown in (a) of drawing 4, the direct current offset voltage of the digital signal inputted presupposes that it went up to step form. As the output signal of the level shifter 12 is also shown in (b) of the figure according to this, an ascending change is carried out, and as the output voltage of the minimum value detecting circuit 17 in the maximum detector circuit 16 of the intermediate voltage detector circuit 15 is also shown in (c) of the figure, and (d), it changes to step form.
[0047]For this reason, as the middle voltage Vo to the subtractor 22 is also shown in (e) of the figure, it changes to step form, and the output of the subtractor 22 changes in the minus direction a lot, as shown in (f) of the figure.
[0048]Therefore, from the low pass filter 23, as shown in (g) of the figure, the error signal Ve

which descends at the speed according to the damping time constant is outputted.
[0049]For this reason, since the shift amount of the level shifter 12 also increases to the minus side at ****, the mean value of the digital signal inputted into the comparator 20 changes in the direction which is in agreement with the threshold voltage Vr, as shown in (b) of the figure.
[0050]As a result, in time t_2, the difference between the input voltage of the subtractor 22 is set to about 0, this stable state is continued henceforth, and the digital signal by which waveform shaping was carried out certainly is acquired from the output of the comparator 20.
[0051]Henceforth, even if offset of an input digital signal changes, since feedback control is always carried out in the direction approaching the threshold voltage Vr, positive waveform-shaping operation stabilizes for it and continues the middle voltage of the digital signal inputted into a comparator.
[0052]
[The 2nd example] Although the control loop for controlling the shift amount of the level shifter 12 was always closed in said 1st example, After stabilizing the shift amount to an input digital signal and becoming an appropriate amount, while holding this shift amount and opening a loop, it can also constitute so that detection operation of the intermediate voltage detector circuit 15 connected to the signal line may be stopped.
[0053]Drawing 5 shows the composition of this hold type waveform shaping circuit 10' which is the 2nd example. The hold circuit 25 where this waveform shaping circuit 10' holds the size of an error signal in response to a hold signal (stop signal), It has the switches 26 and 27 (means for stopping) which close with a hold signal (stop signal) and give reverse-bias-voltage**V_2 to the diodes 16a and 17a of the minimum value detecting circuit 17 in the maximum detector circuit 16.
[0054]In waveform shaping circuit 10' constituted in this way. If the shift amount of the level shifter 12 to an input digital signal inputs a hold signal (stop signal) after turning into an appropriate amount by said same loop control, The value of the error signal Ve which gives a proper shift amount is held by the hold circuit 25, and the shift amount of the level shifter 12 is fixed to an appropriate amount. Since the diodes 16a and 17a of both the detector circuits 16 and 17 of the intermediate voltage detector circuit 15 are electrically separated by reverse bias voltage from the line of a digital signal at this time, the adverse effect (aggravation of a high frequency characteristic) of diode connection to this line can be prevented.
[0055]Although the hold signal explained the case where reverse bias voltage**V_2 was only impressed to the maximum detector circuit 16 and the minimum value detecting circuit 17, in waveform shaping circuit 10' shown in drawing 5, Like the intermediate voltage detector circuit 15 which showed drawing 3 the example, when the very small current of the forward direction is being added from the constant current sources 16c and 17c to the diodes 16a and 17a, a hold signal may be made to perform a change with this constant current source and reverse-bias-voltage**V_2.
[0056]Drawing 6 shows the concrete circuitry of the stop circuit 29 which stops detection operation of the intermediate voltage detector circuit 15 by switching the constant current sources 16c and 17c and reverse-bias-voltage**V_2.
[0057]This stop circuit 29 switches switch 26' and 27' to a hold / limiting circuit mode from a normal mode, in response to the fact that [the above-mentioned hold signal] as a stop signal. In a normal mode, since [said] very small forward bias current is similarly supplied from the constant current sources 16c and 17c, the intermediate voltage detector circuit 15 performs detection of the maximum of the digital signal from the level shifter 12, and the minimum to the

diodes 16a and 17a.
[0058]In a hold mode, since reverse-bias-voltage**V_2 larger (for example, about 4 volts) enough than the maximum of an input digital signal and the minimum is added to the diodes 16a and 17a, the intermediate voltage detector circuit 15 suspends the detecting operation of the maximum and the minimum.
[0059]in limiting circuit mode -- the forward voltage drop of the diodes 16a and 17a -- receiving an input digital signal, since about 1.3 volts reverse-bias-voltage**V_2 which expected 0.7 volt per part is added to the diodes 16a and 17a -- about -- a limiting circuit can be applied by **2V.
[0060]As mentioned above, by carrying out variable control of the voltage set up as reverse-bias-voltage**V_2 in the circuit of drawing 6, so that it may become 4 volts or 1.3 volts according to the state at that time, It can be used with an above-mentioned normal mode, being able to switch both a hold mode or limiting circuit mode. In drawing 6, the numerals 16d and 17d are buffer amplifier, respectively.
[0061]If the stop circuit 29 is constituted as shown in drawing 7, it will become possible to carry out limiter operation of the diodes 16a and 17a in any [of the above-mentioned normal mode and a hold mode] case.
[0062]In the stop circuit 29 shown in drawing 7, about 0.6 volt reverse-bias-voltage**V_3 is always impressed via the diodes 30 and 31 to the diodes 16a and 17a. The constant current source 17c by the side of the minimum value detecting circuit 17 is connected to the hold side of switch 26' by the side of the maximum detector circuit 16, and the constant current source 16c by the side of the maximum detector circuit 16 is connected to the hold side of switch 27' by the side of the minimum value detecting circuit 17.
[0063]For this reason, at the time of a normal mode, it is the same as that of the case of the circuit of said drawing 6 that the forward bias from each constant current source 16c and 17c is applied to the diodes 16a and 17a, and the maximum to an input digital signal and minimum detection are performed.
[0064]However, in this normal mode, if the output voltage from the level shifter 12 becomes lower than -2V, since the diode 17a and the diode 31 of the minimum value detecting circuit 17 flow, the minimum value detecting circuit 17 side will require a limiting circuit in -2V ($-V_3$-1.4V).
[0065]In a normal mode, since the diode 16a and the diode 30 by the side of the maximum detector circuit 16 will flow if the output voltage from the level shifter 12 becomes higher than +2V, the maximum detector circuit 16 side will require a limiting circuit in +2V ($+V_3$+1.4V).
[0066]Above -1.4V is a part for the voltage drop in the diodes 17a and 31, and +1.4V is a part for the voltage drop in the diodes 16a and 30.
[0067]In the time of a hold mode, as for the diodes 16a and 17a, the maximum to an input digital signal and minimum detecting operation are suspended by the constant current source 17c and the reverse bias from thec [16] side, respectively.
[0068]However, in this hold mode, if it is set as about **V_1=**1.3V, If the output voltage from the level shifter 12 becomes lower than -2V or it becomes higher than +2V, a limiting circuit will come to start in -2V or +2V like the time of the normal mode mentioned above, respectively.
[0069]As the above mentioned hold circuit 25 of drawing 5, drawing 6, and drawing 7, as shown in drawing 8, a digital type hold circuit other than an analog type hold circuit can also be used.
[0070]The hold circuit 25 shown in drawing 8 changes the error signal Ve from the control circuit 21 into digital value with A/D converter 32, and memorizes digital value when a hold signal (switching signal) is inputted to the memory circuit 33. The digital value memorized by

the memory circuit 33 is changed into analog voltage by D/A converter 34, and is outputted to the level shifter 12 via the switch 35 by it.
[0071]The switching circuit 35 outputs the error signal from the control circuit 21 to the level shifter 12 as it is, when the hold signal is not inputted, and when the hold signal is inputted, it outputs the signal from D/A converter 34. In order that there may be no change of a hold output compared with an analog type hold circuit, such a digital type hold circuit is advantageous when prolonged hold operation is required.
[0072]Although the subtractor 22 and the low pass filter 23 were made another composition as a concrete circuit of the control circuit 21 in said explanation, as shown in drawing 9, a control circuit can also be simplified using the found the integral type circuit which returns the output of the operational amplifier 21a by the capacitor 21b.
[0073]In said example to know the shift amount in the level shifter 12. If the size of the error signal Ve is read with a voltmeter, or the difference of the average direct current voltage during input and output of the level shifter 12 detected in the integration circuit of resistance R_5 and capacitor C_5, respectively is read with the voltmeter 37 as shown in drawing 10, the shift amount of the level shifter 12 can be known. The threshold level of an input digital signal can be known from this level shift quantity. Since the shift amount in the level shifter 12 can be detected with A/D converter 32 when the digital type hold circuit 25 shown in drawing 8 is used, a circuit like drawing 10 is unnecessary.
[0074]Although said example explained the waveform shaping circuit used by ultrahigh frequency, it can apply the waveform shaping circuit of this invention also to the waveform shaping circuit of a low frequency band.
[0075]As a comparator, what [not only] comprised gallium arsenide type FET of said example but the comparator which comprised a silicon bipolar transistor and a hetero-bipolar transistor (HBT), for example may be used. Various things, such as a level shifter which comprised a blocking capacitor and high frequency blocking coil other than the composition of said example also about the level shifter, can be used.
[0076]
[The 3rd example] Next, the digital-signal-analysis device using the above waveform shaping circuits is explained.
[0077]Drawing 11 is a block diagram showing the composition at the time of mistaking the digital-signal-analysis device of this invention, and applying to a measuring device as the 3rd example.
[0078]After this error measuring device shapes in waveform the data signal under test inputted with a clock signal, It is constituted so that it may compare with the data of the reference signal equivalent to the digital signal into which it identified to the timing in sync with the clock signal into which the binary judging was inputted, and the identified signal was inputted.
[0079]A data signal under test is inputted into the waveform shaping circuit 10 of drawing 1 and the waveform shaping circuit 50 of an identical configuration which were mentioned above.
[0080]That is, the termination of the data signal under test inputted from the input terminal 51 is carried out by input-resistance R_0 (for example, 50ohms), and it is inputted into the level shifter 52. The level shifter 52 changes the direct-current average (offset) voltage of the inputted data signal under test according to the size of the error signal Ve.
[0081]The output of the level shifter 52 is inputted into the intermediate voltage detector circuit 55 and the comparator 60. The intermediate voltage detector circuit 55 the high-level peak voltage of a digital signal and the peak voltage of a low level which are outputted from the level

shifter 52, It detects in the high-level peak detection circuit (maximum detector circuit) 56 and the low-level peak detection circuit (minimum value detecting circuit) 57, respectively, and the middle voltage Vo is outputted from the middle point of two equal resistance R.
[0082]This middle voltage Vo is inputted into the 1st control circuit 61 with the reference voltage (threshold voltage) Vr from the reference voltage generator 59.
[0083]The 1st control circuit 61 that is the 1st control means, The low pass filter which outputs the error signal Ve which integrated with and obtained the subtraction output of the subtractor circuit 62 which detects the difference of the reference voltage Vr and the middle voltage Vo, and the subtractor circuit 62. (It is hereafter described as LPF) It comprises 63 and the middle voltage Vo carries out feedback control of the shift amount of the level shifter 52 in the direction which always approaches the reference voltage Vr.
[0084]High level and when low [the digital signal outputted from the level shifter 52 is higher than the reference voltage Vr and], it outputs the digital signal of a low level, and the comparator 60 shapes the inputted digital signal in waveform.
[0085]As mentioned above, the above composition shall completely be the same as that of the waveform shaping circuit 10 shown in drawing 1, and shall be based on the above-mentioned explanation about the details and the modification of each part.
[0086]On the other hand, the clock signal inputted into the input terminal 70 is inputted into the error test section 75 which are the discrimination circuit 72 and an error measuring instrument via the variable delay device 71. The variable delay device 71 is delayed according to a control signal in the clock signal inputted, and changes relatively the phase of the clock signal over a data signal under test. As this variable delay device 71, the thing of variable-length slab line structure which changes that delaying amount is used as an object for ultrahigh frequency by carrying out slag variable [of the signal line length].
[0087]The discrimination circuit 72 carries out a binary judging in the timing of the standup (or falling) of the clock signal into which the level of the digital signal outputted from the comparator 60 is inputted from the variable delay device 71, and outputs the discernment output to the error test section 75.
[0088]The error test section 75 which is a data analysis part of the error measuring device by this example is constituted by the criterion data generator 76, the code comparison machine 77, the inharmonious counter 78, and the clock counter 79.
[0089]The criterion data generator 76 outputs the criterion data of the same pattern as the data which it is going to measure to the code comparison machine 77 to the timing in sync with the clock signal from the variable delay device 71.
[0090]The code comparison machine 77 of numerals of the output of the discrimination circuit 72 and criterion data corresponds, judges disagreement, and when inharmonious, it outputs a dissidence signal to the inharmonious counter 78.
[0091]While having received the gating signal from the control section 80 mentioned later, the inharmonious counter 78 continues calculation of a dissidence signal, and is performed. The clock counter 79 calculates the clock signal outputted from the variable delay device 71, while having received the gating signal from the control section 80.
[0092]The control section 80 which is the 2nd control means of this error measuring device comprises a microprocessor (CPU) etc., and mainly has two mode management.
[0093]That is, the 1st mode management is the usual measuring process which reads the counting result of both counters, calculates a digital error rate, and displays the result on the display for indication 81, after carrying out predetermined time calculation of the inharmonious

counter 78 and the clock counter 79 simultaneously. The 2nd mode management is the optimal delaying amount detection processing which detects the delaying amount from which carries out prescribed range per-continuum variable [of the delaying amount to the clock signal of the variable delay device 71], and asks for the error rate data to the delaying amount, it memorizes in the memory 80a, and an error rate serves as the minimum before a measuring process.
[0094]A/D converter 65 in drawing 11 changes the error signal Ve from the 1st control circuit 61 of the waveform shaping circuit 50 into digital value, and outputs this value to the control section 80 as a shift amount of the level shifter 52. The control section 80 memorizes this shift amount in the memory 80a, or displays it on the display for indication 81.
[0095]Next, operation of this error measuring device is explained.
[0096]If a data signal under test and a clock signal are inputted into the input terminals 51 and 70, respectively, the waveform shaping circuit 50 will control a shift amount in the direction which coincides the middle voltage Vo of the high level of the inputted data signal under test, and a low level with the reference voltage Vr.
[0097]This operation is completely the same as the operation explained by above-mentioned drawing 4.
[0098]For this reason, from the comparator 60, as shown in (a) of drawing 12, waveform shaping is carried out on the threshold voltage (reference voltage) Vr, and the data signal under test which does not have fluctuation in an amplitude direction is outputted.
[0099]It can be checked by displaying the shift amount from A/D converter 65 on the display for indication 81, or performing the stable decision processing for oneself [control-section 80] that the shift amount of the level shifter 52 has been stabilized.
[0100]Next, the control section 80 performs the optimal delaying amount detection processing mentioned above.
[0101]That is, the control section 80 asks for the cycle T of a clock signal from the counting result, after inputting a gating signal into the predetermined time clock counter 79. And changing the delaying amount of the variable delay device 71 from initial value D_0 to one cycle of a clock signal at least at the predetermined step d, as shown in (b_1) of drawing 12, (b_2), and (b_3), an error rate is searched for for every predetermined step, and the result is memorized in the memory 80a.
[0102](c) of drawing 12 shows change of the error rate over change of the delaying amount memorized by the memory 80a. As opposed to the output signal ((a) of the figure) of the comparator 60 which has fluctuation in a phase constituent so that clearly from this figure, Change of an error rate when the standup timing of a clock signal is changed by 1.5 cycles from (b_1) of the figure to (b_3) of the figure serves as the maximum at the change state point of the output signal of the comparator 60, and two places of the maximum points are obtained.
[0103]The control section 80 sets automatically mean value $D_4$of delaying amount D2 [from which an error rate serves as the maximum], and D6 as the variable delay device 71 as optimal delaying amount that has the phase margin most based on the data of the memorized error rate.
[0104]After performing the above setting out, the control section 80 performs the usual error measuring process, and displays the measured error rate on the display for indication 81 one by one.
[0105]The threshold level of the data signal under test computed from the reference voltage Vr to level shift quantity, and this level shift quantity and comparator 60 from A/D converter 65 is also displayed on the display for indication 81 at any time.
[0106]Although the subtraction result of middle voltage and reference voltage was inputted into the level shifter 52 via LPF63 in the error measuring device of this 3rd example, As shown in

drawing 13, digital conversion of the subtraction result is carried out to subtraction data with A/D converter 65, A shift amount for this subtraction data to approach zero may be computed by the operation control part 90, and this computed shift amount data may be sent out to D/A converter 66, and it may constitute so that the shift amount of the level shifter 52 may be controlled. This operation control part 90 is constituted by one CPU with the control section 80.
[0107]The A/D conversion of the middle voltage outputted from the intermediate voltage detector circuit 55 is carried out directly, It is also possible to constitute so that it may send to the operation control part 90 and shift amount data corresponding this intermediate voltage data to that difference as compared with reference voltage data may be outputted to the level shifter 52 via D/A converter 65 by the operation control part 90. In this case, the operation control part 90 serves as the 1st control means.
[0108]In said 3rd example, in order to set up the optimal delaying amount to a clock signal, had determined the optimum value from the maximum of the error rate acquired by changing a delaying amount over the above by one cycle of a clock signal, but. It may be made for an error rate to set up the delaying amount used as the minimum as an optimum value as it is. This is an effective method, when fluctuation of the phase of an input appearance signal is large and the flat part between $D_{of\ (c)5from\ D3\ of\ drawing\ 12}$ is very narrow.
[0109]It may be made to set up the mean value of two delaying amounts (for example, D_3 of drawing 12, D_5) which give the greatest not an error rate but equal error rate like said example as optimal delaying amount.
[0110]By operating the input means of the switch etc. which were formed in the display for indication, After starting a series of operations which set up the optimal threshold voltage of a data signal under test and completing the operation, operation which sets up the optimal delaying amount is performed and it may be made to display the threshold level and the delaying amount which were set up on a display for indication.
[0111]In said 3rd example, although the phase by the side of a clock signal was delayed, this may not limit this invention, and as shown, for example in drawing 14, it may form the variable delay device 71 between the input terminal 51 by the side of a data signal under test, and the level shifter 52. The variable delay device 71 may be formed between the level shifter 52 and the comparator 60 or between the comparator 60 and the discrimination circuit 72.
[0112]Although the waveform shaping circuit 10 shown in drawing 1 and the waveform shaping circuit 50 of the identical configuration were performing waveform shaping of the input signal in said 3rd example, Waveform shaping circuit 10' of the 2nd example (drawing 5) which has a hold facility of a shift amount and an operation stop function of the intermediate voltage detector circuit 55 may be used. The circuit which has the limiter function similarly shown in above-mentioned drawing 6 as a modification of drawing 5 and drawing 7 may be used.
[0113]The circuit of drawing 13 mentioned above may be transformed still like drawing 15, and the digital type hold circuit explained by above-mentioned drawing 8 may be formed.
[0114]It judges itself that the loop of the waveform shaping circuit 50 was stabilized as for the operation control part 90 of this composition, and it became the optimal shift amount, While outputting a hold signal (stop signal) to the switching circuit 35 and the stop circuit 69 and carrying out fixed setting out of the optimal shift amount to the level shifter 52, the detecting operation of the intermediate voltage detector circuit 55 is stopped (in addition, the stop circuit 69 consists of the same composition as the above-mentioned stop circuit 29).
[0115]The operation control part 90 which performs setting-out control of the optimal shift amount to the level shifter 52, and stop control of intermediate voltage detecting operation in this

way, If the control section 80 which performs setting-out control of the optimal delaying amount to the variable delay device 71 is constituted from one CPU, A series of programs can be made to perform the setting processing of the optimal shift amount and the setting processing of the optimal delaying amount continuously, [as opposed to a data signal under test by easy key operation etc.] And there is an advantage that transfer of data with other devices can be easily performed using the communication function of CPU.

[0116]Drawing 16 is an example of the device which shows the more concrete example of the error measuring device of the 3rd example of this invention, and performs error measurement of the data signal of ultrahigh frequency under test especially.

[0117]In drawing 16, the input clock applied to the input data applied to the waveform shaping circuit 101 and the variable delay device 102 is rationalized as mentioned above, respectively, and it is outputted to the discrimination circuit 103.

[0118]The data in which discernment which was mentioned above by this discrimination circuit 103 was made is demultiplexed by 1/N in the 1/N demultiplexer 104 with the 1/N clock by which it is generated from the timing generation part 105 based on the output clock of the variable delay device 102. For example, in the case of N= 32, input data is demultiplexed by 310 MHz at 10 GHz, and error detection of the input data is carried out by the error detection part 106 as 32-channel data. this error result -- an error -- calculation -- it is sent to the indicator 108 and the synchronous controlling part 109 via the part 107. The reference pattern generating part 110 generates the standard pattern information for giving the error detection part 106 according to the output from this synchronous controlling part 109.

[0119]this error detection part 106, the reference pattern generating part 110, and an error -- calculation -- the part 107 and the synchronous controlling part 109 are controlled by the 1/N clock from the timing generation part 105. The control section 111 which comprises a CPU controls each part. The auto search part 112 controls the waveform shaping circuit 101 and the variable delay device 102 in the respectively proper state as well as said each example under control of the control section 111.

[0120]In this error measuring device, since the data signal identified to the optimal timing is divided into the parallel data of the speed of 1/N and an error judging is carried out by the discrimination circuit 103 like said example, error measurement of the data signal of ultrahigh frequency can be ensured.

[0121]The above-mentioned example is applicable like other digital analysis devices, such as a logic analyzer, although the example which mistook the digital-signal-analysis device of this invention, and was applied to the measuring device was explained.

[0122]

[Effect of the Invention]As explained above, the waveform shaping circuit of this invention, The direct current offset voltage of an input digital signal, i.e., the middle voltage of the high-level voltage of the output signal of a level shifter, and low-level voltage. The shift amount of a level shifter is controlled in the direction put close to a predetermined threshold, and it is constituted so that the output signal of the level shifter may be shaped in waveform with a predetermined threshold.

[0123]For this reason, without carrying out troublesome waveform observation and hand regulation, the center of the amplitude of the digital signal inputted into a comparator is driven into the state where it was always in agreement with the predetermined threshold, and positive waveform shaping can be performed.

[0124]A shift amount can be fixed to an appropriate amount and it is effective in not worsening

the high frequency characteristic of a signalling channel in the holding circuit holding the size of the error signal over a level shifter, and the waveform shaping circuit in which the means for stopping which stops operation of an intermediate voltage detector circuit was provided.
[0125]Based on the error measurement result obtained by the digital-signal-analysis device of this invention carrying out prescribed range delay variable [of the phase of the digital signal and clock signal which are outputted from said waveform shaping circuit] relatively like said explanation, A delaying amount for the timing of discernment to go into the optimal position between the change state points that the digital signal inputted into a discrimination circuit adjoins each other is detected from a comparator, and it is constituted so that the delaying amount may be set as a variable delay device.
[0126]For this reason, the operating point and identification timing of waveform shaping by a comparator can be set as an optimum state in the state where there are no wave-like error and individual difference by disorder, without carrying out the voltage adjustment and phase adjustment operation by complicated hand control while carrying out waveform observation.

TECHNICAL FIELD

[Industrial Application]This invention relates to the digital-signal-analysis device which analyzes the waveform shaping circuit which shapes in waveform and outputs the digital signal inputted, and the digital signal inputted like a logic analyzer or an error measuring device synchronizing with a clock signal.

EFFECT OF THE INVENTION

[Effect of the Invention]As explained above, the waveform shaping circuit of this invention, The direct current offset voltage of an input digital signal, i.e., the middle voltage of the high-level voltage of the output signal of a level shifter, and low-level voltage. The shift amount of a level shifter is controlled in the direction put close to a predetermined threshold, and it is constituted so that the output signal of the level shifter may be shaped in waveform with a predetermined threshold.
[0123]For this reason, without carrying out troublesome waveform observation and hand regulation, the center of the amplitude of the digital signal inputted into a comparator is driven into the state where it was always in agreement with the predetermined threshold, and positive waveform shaping can be performed.
[0124]A shift amount can be fixed to an appropriate amount and it is effective in not worsening the high frequency characteristic of a signalling channel in the holding circuit holding the size of the error signal over a level shifter, and the waveform shaping circuit in which the means for stopping which stops operation of an intermediate voltage detector circuit was provided.
[0125]Based on the error measurement result obtained by the digital-signal-analysis device of this invention carrying out prescribed range delay variable [of the phase of the digital signal and clock signal which are outputted from said waveform shaping circuit] relatively like said explanation, A delaying amount for the timing of discernment to go into the optimal position between the change state points that the digital signal inputted into a discrimination circuit adjoins each other is detected from a comparator, and it is constituted so that the delaying amount may be set as a variable delay device.
[0126]For this reason, the operating point and identification timing of waveform shaping by a

comparator can be set as an optimum state in the state where there are no wave-like error and individual difference by disorder, without carrying out the voltage adjustment and phase adjustment operation by complicated hand control while carrying out waveform observation.

TECHNICAL PROBLEM

[Description of the Prior Art]Generally, after shaping in waveform the digital signal inputted from the outside by the waveform shaping circuit which comprises a comparator, it comprises digital-signal-analysis devices mentioned above, such as a logic analyzer and an error measuring device, so that the binary judging may be performed.
[0003]It is necessary to set it as the best operating point which corresponds to offset of the digital signal into which the operating point of a comparator is inputted, and is not influenced by a noise in this kind of waveform shaping circuit. In order to set up this operating point, either of the following three methods was carried out conventionally.
[0004](1) The technique of setting the threshold level (reference voltage) to a comparator as an optimum state manually, while monitoring the output wave of a comparator.
[0005](2) A technique make the digital signal inputted input into a comparator via a capacitor, and excluding the influence of offset.
[0006](3) A technique which carries out manual variable by a level shifter beforehand supposing the direct-current average level of the digital signal inputted, and is inputted into a comparator.
[0007]However, in (1) or (3) technique mentioned above, whenever operating point setting out by hand control is troublesome and the level of an input signal and offset change, the setting-operation must be performed.
[0008]In the technique of (2) mentioned above, the threshold which the offset voltage of the digital signal inputted into a comparator according to the mark rate (ratio of the total number of bits to generate and the number of marks contained in it) of the digital signal inputted changed and fixed cannot perform positive waveform shaping.
[0009]For this reason, the technique inputted into a comparator by making high-level voltage of the digital signal inputted and intermediate voltage of low-level voltage into a threshold is also considered.
[0010]However, in the case of the comparator of the large comparison low speed of a common mode input range, this technique is effective, but. Like the comparator for shaping the signal of ultrahigh frequency (several gigahertz) in waveform, when a common mode input range is very narrow, the comparator itself is saturated by change of the offset voltage of an input signal, and there is a problem that normal waveform-shaping operation cannot be performed.
[0011]On the other hand, the binary judging of the digital signal which shaped in waveform is performed, and the digital-signal-analysis device which analyzes the digital data is constituted as shown in drawing 17 from the former.
[0012]That is, waveform shaping of the data signal under test inputted into one input terminal 1 is carried out by the comparator 3 which makes a threshold reference voltage Vr from the reference voltage generator 2. Since this reference voltage Vr is beforehand set as the best value by either of the techniques mentioned above, the fluctuation ingredient of the amplitude direction of the data signal under test shown in (a) of drawing 18, As shown in (b) of the figure, waveform shaping is carried out, and it is inputted into data input terminal D of the discrimination circuit 4 which comprised a D type flip-flop.
[0013]The clock signal inputted into the input terminal 5 of another side is inputted into clock

terminal CP of the discrimination circuit 4 via the variable delay device 6.
[0014]This variable delay device 6 is beforehand adjusted so that a clock signal may rise to the timing whose binary level of the data signal inputted into the discrimination circuit 4 is most stable.
[0015]The output signal of the comparator 3 shown in (b) of drawing 18 as this adjustment, displaying the clock signal shown in (c) of the figure on a dual trace oscilloscope -- the standup timing of a clock signal -- the change state points I and II of a digital signal -- so that it may be located mostly at the halfway point (point that the phase margin is the largest), The method of adjusting the delaying amount of the variable delay device 6 with hand control was taken conventionally.
[0016]Thus, discernment of a binary is made to the standup timing of a clock signal of inputting the digital signal from the comparator 3 into the discrimination circuit 4, the decision output is inputted into the data analysis part 7 with a clock signal, and predetermined data analysis is conducted.
[0017]However, in such a conventional digital-signal-analysis device of composition, in addition to the hand regulation of the waveform shaping circuit mentioned above, hand regulation of the delaying amount also had to be performed, it was easy to produce the difference of these preset values according to the operator's individual difference, and there was a problem that a difference will appear also in an analysis result.
[0018]When adjusting by carrying out waveform observation with an oscilloscope, connection between apparatus is not only complicated, but by connection of an oscilloscope, the waveform of a signal may be confused and it may cause malfunction. As especially mentioned above, in connecting the cable for waveform observation to the signal of ultrahigh frequency (several gigahertz), adjustment with it becomes difficult. [this wave-like large disorder and] [exact]
[0019]For this reason, although the technique of providing the monitor terminal for waveform observation was also in the digital-signal-analysis device, there was no change in always having to prepare apparatus for waveform observation, such as an oscilloscope, and it was dramatically inconvenient.
[0020]An object of this invention is to provide the waveform shaping circuit and digital-signal-analysis device which solved the problem mentioned above.

MEANS

[Means for Solving the Problem]In order to solve said SUBJECT, a waveform shaping circuit of this invention, A level shifter (12) which carries out variable control of the direct current offset voltage of an inputted digital signal, A comparator (20) which shapes in waveform and outputs a digital signal outputted from this level shifter as compared with predetermined reference voltage, An intermediate voltage detection means (15) to detect and output middle voltage of high-level voltage of a digital signal and low-level voltage which were outputted from said level shifter, In response to middle voltage and said predetermined reference voltage which are outputted from this intermediate voltage detection means, in order to make said middle voltage equal to said predetermined reference voltage, it has a control means (21) which outputs a control signal to which said direct current offset voltage is changed to said level shifter.
[0022]A level shifter (52) which carries out variable control of the direct current offset voltage of a digital signal into which a digital-signal-analysis device of this invention was inputted, A comparator (60) which shapes in waveform and outputs a digital signal outputted from this level

shifter as compared with predetermined reference voltage, An intermediate voltage detector circuit (55) which detects and outputs middle voltage of high-level voltage of a digital signal and low-level voltage which were outputted from said level shifter, Middle voltage and said predetermined reference voltage which are outputted from this intermediate voltage detector circuit are received, The 1st control means (61) that outputs a control signal to which said direct current offset voltage is changed to said level shifter in order to make said middle voltage equal to said predetermined reference voltage, A variable delay device (71) which changes relatively a phase between an inputted clock signal and an output of said comparator, A discrimination circuit (72) which receives an output and said clock signal of said comparator into which a phase was relatively changed by this variable delay device, and judges numerals of an output signal of a standup of this clock signal, or said comparator at the time of falling, An error measuring instrument (75) which compares a decision signal from this discrimination circuit with a reference signal equivalent to said inputted digital signal, and outputs an error signal, It has the 2nd control means (80) that decreases said error signal which detects an almost middle delaying amount of a delaying amount from which an error signal becomes ******** with the maximum in response to an output of this error measuring instrument, and sends out this middle delaying amount to said variable delay device, and said error measuring instrument outputs.

OPERATION

[Function]Since it is constituted in this way, in the waveform shaping circuit of this invention, the digital signal inputted is inputted into a comparator via a level shifter, and waveform shaping is carried out by predetermined reference voltage. The high-level voltage of the digital signal outputted from a level shifter and the middle voltage of low-level voltage are detected by an intermediate voltage detection means, and are outputted to a control means with reference voltage. A control means outputs a control signal for middle voltage to become equal to reference voltage to a level shifter, and changes the direct current offset voltage of the digital signal inputted.

[0024]In the digital-signal-analysis device of this invention, a phase in the meantime is changed by the variable delay device, and the clock signal inputted from the output signal and input terminal of the comparator by which waveform shaping was carried out in the waveform shaping circuit of the above-mentioned invention and the waveform shaping circuit of the identical configuration is inputted into a discrimination circuit. The decision signal from a discrimination circuit is compared with the reference signal which is equivalent to the inputted digital signal with an error measuring instrument. The error signal detected by the error measuring instrument is inputted into the 2nd control means. the delaying amount from which the delaying amount of a variable delay device is changed, and an error signal becomes ******** with the maximum while the 2nd control means receives the error signal from an error measuring instrument -- a middle delaying amount is detected mostly and it outputs to a variable delay device.

EXAMPLE

[Example]Hereafter, the 1st example of this invention is described based on a drawing.

[0026]Drawing 1 is a circuit diagram showing the composition of the waveform shaping circuit 10 of the 1st example.

[0027]In drawing 1, the termination of the input digital signal inputted into the terminal 11 is

carried out by input-resistance R_0 (for example, 50ohms), and it is inputted into the level shifter 12.

[0028]The level shifter 12 changes the average direct-current (offset) voltage level of an input digital signal according to the size of the error signal (control signal) Ve from the control circuit 21 mentioned later. For this reason, the level shifter 12 is constituted as shown, for example in drawing 2.

[0029]That is, the average direct current voltage of an input digital signal is detected in the integration circuit by resistance R_1 and capacitor C_1, and is inputted into the adding machine 13. The adding machine 13 adds the error signal Ve to this average direct current voltage, and outputs that added voltage via resistance R_2. Between resistance R_2 and the terminal 11, capacitor C_2 which passes only the alternating current component of an input digital signal is provided. Therefore, from the node of capacitor C_2 and resistance R_2, the signal with which the level was shifted only for the error voltage Ve is outputted to the signal with which the output voltage from the adding machine 13 was applied to the alternating current component of an input digital signal, i.e., an input digital signal.

[0030]Resistance R_1 and R_2 have the high resistance about [which does not have influence in the transmission impedance of 50 ohms] number 10Komega.

[0031]The output of the level shifter 12 is inputted into the intermediate voltage detector circuit 15 and the comparator 20 mentioned later as shown in drawing 1.

[0032]The maximum detector circuit 16 where the intermediate voltage detector circuit 15 detects the maximum voltage of the output signal of the level shifter 12, It is constituted by the intermediate voltage output circuit 18 which outputs the middle voltage between the output voltage of the minimum value detecting circuit 17 which detects the minimum voltage of the output signal of the level shifter 12, and both the detector circuits 16 and 17 from the node of two resistance R_3 of the same resistance by which the series connection was carried out mutually, and R_4.

[0033]The comparator 20 outputs high level, when the level of the output signal of the level shifter 12 inputted into one input terminal IN is larger than the predetermined reference voltage (henceforth threshold voltage) Vr applied to the input terminal REF of another side, and when small, it outputs the digital signal of a low level. This comparator 20 comprises a semiconductor device for ultrahigh frequency (for example, gallium arsenide type FET), etc.

[0034]The middle voltage Vo outputted from the intermediate voltage detector circuit 15 and the threshold voltage Vr are inputted into the control circuit 21 which is a control means of this waveform shaping circuit 10. The control circuit 21 detects the difference of the middle voltage Vo and the threshold voltage Vr which are inputted with the subtractor 22, and outputs the difference voltage signal to the level shifter 12 via the low pass filter 23, The middle voltage Vo controls the shift amount of the level shifter 12 in the direction which is in agreement with the threshold voltage Vr.

[0035]Drawing 3 shows an example of the more concrete circuit of the intermediate voltage detector circuit 15 and the control circuit 21.

[0036]Namely, the diode 16a by which the anode side was connected to the output of the level shifter 12 in the maximum detector circuit 16, It has the Masakata-oriented peak detection circuit formed by the capacitor 16b connected with the cathode of the diode 16a between groundings, Between the node of this diode 16a and capacitor 16b, and predetermined negative supply-V_1, the constant current source 16c which sends very small forward bias current is connected to the diode 16a.

[0037]The diode 17a by which the cathode side was connected to the output of the level shifter

12 in the minimum value detecting circuit 17, It has a peak detection circuit of the negative direction formed by the capacitor 17b connected between the anode side of the diode 17a, and grounding, Between the node of the diode 17a and the capacitor 17b, and predetermined positive supply $+V_1$, the constant current source 17c which sends very small forward bias current is connected to the diode 17a.

[0038]Therefore, from the node of the diode 16a of the maximum detector circuit 16, and the capacitor 16b, The high-level voltage more than negative supply-V_1 voltage will be outputted among the digital signals outputted from the level shifter 12, and the low-level voltage below positive supply $+V_1$ voltage will be outputted from the node of the diode 17a of the minimum value detecting circuit 17, and the capacitor 17b.

[0039]The forward bias current from the constant current sources 16c and 17c over each diodes 16a and 17a hardly affects it to an input digital signal, but is set as the current value about [required to compensate the nonlinearity of detection operation of each diodes 16a and 17a moreover] 1microA.

[0040]The capacity value of the capacitors 16c and 17c is set as the value of about 1000 PF which can hold the peak value of the digital signal of 1 kHz or more of cycle periods in consideration of the forward bias current over each diodes 16a and 17a being a 1microA grade.

[0041]The subtractor 22 of the control circuit 21 is formed of the differential amplifier 22a and the feedback resister 22b, and the voltage according to the difference of the intermediate voltage Vo and the threshold voltage Vr is outputted from the differential amplifier 22a. The low pass filter 23 formed by the resistance 23a and the capacitor 23b outputs the error signal Ve excluding the noise component from the output of the differential amplifier 22a to the level shifter 12.

[0042]Therefore, since the output voltage of the differential amplifier 22a will rise if the middle voltage Vo falls to the threshold voltage Vr, the level of the digital signal which the error signal Ve goes up and is outputted from the level shifter 12 goes up to the whole. Conversely, since the output voltage of the differential amplifier 22a will decline if the middle voltage Vo rises to the threshold voltage Vr, the level of the digital signal which the error signal Ve falls and is outputted from a level shifter will fall to the whole.

[0043]Next, operation of the above-mentioned waveform shaping circuit 10 is explained.

[0044]Now, temporarily, the maximum of the digital signal inputted to the level shifter 12 by time t_0 and the mean value of the minimum presuppose that it is equal to the threshold voltage Vr of the comparator 20, as shown in (a) of drawing 4.

[0045]In this case, since the output of the subtractor 22 of the control circuit 21 serves as zero, the digital signal inputted into the level shifter 12 is inputted into the comparator 20 as it is, and waveform shaping is carried out on the threshold voltage Vr.

[0046]And in time t_1, as shown in (a) of drawing 4, the direct current offset voltage of the digital signal inputted presupposes that it went up to step form. As the output signal of the level shifter 12 is also shown in (b) of the figure according to this, an ascending change is carried out, and as the output voltage of the minimum value detecting circuit 17 in the maximum detector circuit 16 of the intermediate voltage detector circuit 15 is also shown in (c) of the figure, and (d), it changes to step form.

[0047]For this reason, as the middle voltage Vo to the subtractor 22 is also shown in (e) of the figure, it changes to step form, and the output of the subtractor 22 changes in the minus direction a lot, as shown in (f) of the figure.

[0048]Therefore, from the low pass filter 23, as shown in (g) of the figure, the error signal Ve which descends at the speed according to the damping time constant is outputted.

[0049]For this reason, since the shift amount of the level shifter 12 also increases to the minus side at ****, the mean value of the digital signal inputted into the comparator 20 changes in the direction which is in agreement with the threshold voltage Vr, as shown in (b) of the figure.
[0050]As a result, in time t_2, the difference between the input voltage of the subtractor 22 is set to about 0, this stable state is continued henceforth, and the digital signal by which waveform shaping was carried out certainly is acquired from the output of the comparator 20.
[0051]Henceforth, even if offset of an input digital signal changes, since feedback control is always carried out in the direction approaching the threshold voltage Vr, positive waveform-shaping operation stabilizes for it and continues the middle voltage of the digital signal inputted into a comparator.
[0052]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1]It is a block diagram showing the 1st example composition of this invention.
[Drawing 2]It is a circuit diagram showing an example of the concrete circuit of the important section of drawing 1.
[Drawing 3]It is a circuit diagram showing an example of the concrete circuit of the important section of drawing 1.
[Drawing 4]It is a signal figure for explaining operation of one example.
[Drawing 5]It is a block diagram showing the composition of the 2nd example of this invention.
[Drawing 6]It is a circuit diagram showing the modification of the important section of the 2nd example.
[Drawing 7]It is a circuit diagram showing the modification of the important section of the 2nd example.
[Drawing 8]It is a circuit diagram showing the modification of the important section of the 2nd example.
[Drawing 9]It is a circuit diagram showing the modification of the important section of the 1st and 2nd example.
[Drawing 10]It is a circuit diagram for reading a shift amount directly.
[Drawing 11]It is a block diagram showing the composition of the 3rd example of this invention.
[Drawing 12]It is a figure for explaining operation of the 3rd example.
[Drawing 13]It is an important section block diagram showing the modification of the 3rd example.
[Drawing 14]It is a block diagram showing other modifications of the 3rd example.
[Drawing 15]It is a block diagram showing other modifications of the 3rd example.
[Drawing 16]It is a block diagram showing the important section of the 3rd example more concretely.
[Drawing 17]It is a block diagram showing the composition of a device conventionally.
[Drawing 18]It is a signal figure for explaining operation of a device conventionally.
[Description of Notations]
10 10' Waveform shaping circuit
12 Level shifter
15 Intermediate voltage detector circuit
16 Maximum detector circuit

17 Minimum value detecting circuit
18 Intermediate voltage output circuit
20 Comparator
21 Control circuit
22 Subtractor
23 Low pass filter
25 Hold circuit
26 and 27 Switch
29 Stop circuit
32 A/D converter
33 Memory circuit
34 D/A converter
35 Switch
37 Voltmeter
50 Waveform shaping circuit
52 Level shifter
55 Intermediate voltage detector circuit
60 Comparator
61 The 1st control circuit
65 A/D converter
71 Variable delay device
72 Discrimination circuit
75 Error test section
76 Criterion data generator
77 Code comparison machine
78 Inharmonious counter
79 Clock counter
80 Control section
81 Display for indication
90 Operation control part
101 Waveform shaping circuit
102 Variable delay device
103 Discrimination circuit
104 1/N demultiplexer
105 Timing generation part
106 Error detection part
107 an error -- calculation -- a part
108 Indicator
109 Synchronous controlling part
110 Reference pattern generating part
111 CPU
112 Auto search part

[Translation done.]

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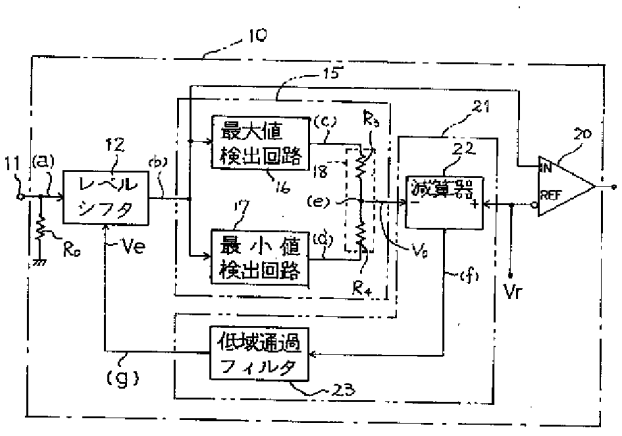
(71)出願人　000000572
アンリツ株式会社
東京都港区南麻布５丁目10番27号
(72)発明者　斉藤　澄夫
東京都港区南麻布五丁目10番27号　アンリツ株式会社内
(74)代理人　弁理士　早川　誠志

(54)【発明の名称】　波形整形回路およびデイジタル信号解析装置

(57)【要約】
【目的】　入力されるディジタル信号を、その振幅変化やオフセットの影響をを受けずに安定に波形整形する。
【構成】　入力されるディジタル信号は、レベルシフタ１２を介して中間電圧検出回路１５へ入力される。中間電圧検出回路１５は、入力されたディジタル信号のハイレベルとローレベルとの中間の電圧V_0を検出して、制御回路２１の減算器２２へ出力する。制御回路２１は、中間の電圧V_0と参照電圧V_rとの差信号を、低域通過フィルタ２５を介してレベルシフタ１２へ出力し、中間の電圧V_0が参照電圧V_rに近づく方向にレベルシフタ１２のシフト量を制御する。レベルシフタ１２によってレベルシフトされたディジタル信号は、参照電圧V_rをしきい値とするコンパレータ２０へ入力されて波形整形される。



【特許請求の範囲】
【請求項１】入力されたディジタル信号の直流オフセット電圧を可変制御するレベルシフタ（１２）と、該レベルシフタから出力されたディジタル信号を所定の参照電圧と比較し、波形整形して出力するコンパレータ（２０）と、前記レベルシフタから出力されたディジタル信号のハイレベル電圧とローレベル電圧との中間の電圧を検出して出力する中間電圧検出手段（１５）と、該中間電圧検出手段から出力される中間の電圧と前記所定の参照電圧とを受けて、前記中間の電圧を前記所定の参照電圧と等しくするために前記直流オフセット電圧を変化させる制御信号を前記レベルシフタに出力する制御手段（２１）とを備えた波形整形回路。
【請求項２】前記制御手段から出力された前記制御信号を保持する保持手段（２５）と、該保持手段によって前記制御信号が保持されたとき、前記中間電圧検出手段の作動を停止させる停止手段（２６）、（２７）とを備えた第１項記載の波形整形回路。
【請求項３】入力されたディジタル信号の直流オフセット電圧を可変制御するレベルシフタ（５２）と、該レベルシフタから出力されたディジタル信号を所定の参照電圧と比較し、波形整形して出力するコンパレータ（６０）と、前記レベルシフタから出力されたディジタル信号のハイレベル電圧とローレベル電圧との中間の電圧を検出して出力する中間電圧検出回路（５５）と、該中間電圧検出回路から出力される中間の電圧と前記所定の参照電圧とを受けて、前記中間の電圧を前記所定の参照電圧と等しくするために前記直流オフセット電圧を変化させる制御信号を前記レベルシフタに出力する第１の制御手段（６１）と、入力されたクロック信号と前記コンパレータの出力との間の位相を相対的に可変する可変遅延器（７１）と、該可変遅延器によって位相が相対的に可変された、前記コンパレータの出力と前記クロック信号とを受けて、該クロック信号の立上りまたは立下り時における前記コンパレータの出力信号の符号を判定する識別器（７２）と、該識別器からの判定信号と前記入力されたディジタル信号に相当する基準信号とを比較して誤り信号を出力する誤り測定器（７５）と、該誤り測定器の出力を受けて相隣り合って誤り信号が最大値となる遅延量のほぼ中間の遅延量を検出して、かつ、この中間遅延量を前記可変遅延器に送出して前記誤り測定器が出力する前記誤り信号を減少させる第２の制御手段（８０）とを備えたディジタル信号解析装置。
【発明の詳細な説明】
【０００１】
【産業上の利用分野】本発明は、入力されるディジタル信号を波形整形して出力する波形整形回路および、ロジックアナライザや誤り測定装置などのようにクロック信号に同期して入力されるディジタル信号を解析するディジタル信号解析装置に関する。
【０００２】
【従来の技術と解決しようとする課題】一般に、前述したロジックアナライザや誤り測定装置等のディジタル信号解析装置では、外部から入力されるディジタル信号を、コンパレータで構成される波形整形回路によって波形整形した後、その２値判定を行なうよう構成されている。
【０００３】この種の波形整形回路では、コンパレータの動作点を、入力されるディジタル信号のオフセットに対応し、且つノイズの影響を受けない最良の動作点に設定する必要がある。この動作点を設定するために、従来は、次の３つの方法のいずれかを実施していた。
【０００４】（１）コンパレータの出力波形をモニタしながらコンパレータに対するしきい値レベル（参照電圧）を手動で最適状態に設定する手法。
【０００５】（２）入力されるディジタル信号をコンデンサを介してコンパレータに入力させてオフセットの影響を除く手法。
【０００６】（３）入力されるディジタル信号の直流平均レベルを予め想定してレベルシフタで手動可変してコンパレータに入力する手法。
【０００７】しかしながら、前述した（１）、（３）の手法では、手動による動作点設定が煩しく、入力信号のレベルやオフセットが変わる毎にその設定動作を行なわなければならない。
【０００８】また、前述した（２）の手法では、入力されるディジタル信号のマーク率（発生する全ビット数とその中に含まれるマーク数との比）に応じてコンパレータに入力されるディジタル信号のオフセット電圧が変化してしまい、固定したしきい値で、確実な波形整形が行なえない。
【０００９】このため、入力されるディジタル信号のハイレベル電圧とローレベル電圧の中間電圧をしきい値としてコンパレータに入力する手法も考えられる。
【００１０】ところが、この手法は、同相入力範囲の広い比較的低速のコンパレータの場合に有効であるが、超高周波（数ＧＨｚ）の信号を波形整形するためのコンパレータのように、同相入力範囲が極めて狭い場合には、入力信号のオフセット電圧の変化によってコンパレータ自身が飽和してしまい、正常な波形整形動作が行なえないという問題がある。
【００１１】一方、波形整形したディジタル信号の２値判定を行なって、そのディジタルデータを解析するディジタル信号解析装置は、従来から図１７に示すように構成されている。
【００１２】即ち、一方の入力端子１に入力される被測定データ信号は、参照電圧発生器２からの参照電圧Ｖｒをしきい値とするコンパレータ３によって波形整形される。この参照電圧Ｖｒは、前述した手法のいずれかによって予め最良の値に設定されているため、図１８の

（ａ）に示す被測定データ信号の振幅方向のゆらぎ成分は、同図の（ｂ）に示すように波形整形されて、Ｄタイプのフリップフロップで構成された識別器４のデータ入力端子Ｄに入力される。

【００１３】また、他方の入力端子５に入力されるクロック信号は可変遅延器６を介して、識別器４のクロック端子ＣＰへ入力される。

【００１４】この可変遅延器６は、識別器４に入力されるデータ信号の２値レベルが、最も安定しているタイミングにクロック信号が立上がるように、予め調整されている。

【００１５】この調整として、図１８の（ｂ）に示したコンパレータ３の出力信号と、同図の（ｃ）に示すクロック信号とを２現象オシロスコープに表示して、クロック信号の立上がりタイミングが、ディジタル信号の状態遷移点Ｉ、IIのほぼ中間点（位相余裕が最も大きい点）に位置するように、可変遅延器６の遅延量を手動により調整する方法が従来よりとられていた。

【００１６】このようにして、コンパレータ３からのディジタル信号は、識別器４に入力されるクロック信号の立上りタイミングで２値の識別がなされ、その判定出力は、クロック信号とともにデータ解析部７へ入力されて、所定のデータ解析がなされる。

【００１７】しかしながら、このような構成の従来のディジタル信号解析装置では、前述した波形整形回路の手動調整に加えて、遅延量の手動調整も行なわなければならず、操作者の個人差によってこれらの設定量の差が生じやすく、解析結果にも差がでてしまうという問題があった。

【００１８】また、オシロスコープで波形観測して調整を行なう場合、機器間の接続が煩雑であるばかりでなく、オシロスコープの接続によって信号の波形が乱れ、誤動作を引き起こすことがある。特に、前述したように超高周波（数ＧＨｚ）の信号に波形観測用のケーブルを接続する場合には、この波形の乱れが大きく正確な調整が困難となる。

【００１９】このため、ディジタル信号解析装置に波形観測用のモニタ端子を設ける手法もあるが、オシロスコープ等の波形観測用機器を常時準備しておかなければならないことに変わりがなく、非常に不便であった。

【００２０】本発明は、前述した問題を解決した波形整形回路およびディジタル信号解析装置を提供することを目的としている。

【００２１】

【課題を解決するための手段】前記課題を解決するために、本発明の波形整形回路は、入力されたディジタル信号の直流オフセット電圧を可変制御するレベルシフタ（１２）と、該レベルシフタから出力されたディジタル信号を所定の参照電圧と比較し、波形整形して出力するコンパレータ（２０）と、前記レベルシフタから出力されたディジタル信号のハイレベル電圧とローレベル電圧との中間の電圧を検出して出力する中間電圧検出手段（１５）と、該中間電圧検出手段から出力される中間の電圧と前記所定の参照電圧とを受けて、前記中間の電圧を前記所定の参照電圧と等しくするために前記直流オフセット電圧を変化させる制御信号を前記レベルシフタに出力する制御手段（２１）とを備えている。

【００２２】また、本発明のディジタル信号解析装置は、入力されたディジタル信号の直流オフセット電圧を可変制御するレベルシフタ（５２）と、該レベルシフタから出力されたディジタル信号を所定の参照電圧と比較し、波形整形して出力するコンパレータ（６０）と、前記レベルシフタから出力されたディジタル信号のハイレベル電圧とローレベル電圧との中間の電圧を検出して出力する中間電圧検出回路（５５）と、該中間電圧検出回路から出力される中間の電圧と前記所定の参照電圧とを受けて、前記中間の電圧を前記所定の参照電圧と等しくするために前記直流オフセット電圧を変化させる制御信号を前記レベルシフタに出力する第１の制御手段（６１）と、入力されたクロック信号と前記コンパレータの出力との間の位相を相対的に可変する可変遅延器（７１）と、該可変遅延器によって位相が相対的に可変された、前記コンパレータの出力と前記クロック信号とを受けて、該クロック信号の立上りまたは立下り時における前記コンパレータの出力信号の符号を判定する識別器（７２）と、該識別器からの判定信号と前記入力されたディジタル信号に相当する基準信号とを比較して誤り信号を出力する誤り測定器（７５）と、該誤り測定器の出力を受けて相隣り合って誤り信号が最大値となる遅延量のほぼ中間の遅延量を検出して、かつ、この中間遅延量を前記可変遅延器に送出して前記誤り測定器が出力する前記誤り信号を減少させる第２の制御手段（８０）とを備えている。

【００２３】

【作用】このように構成されているため、本発明の波形整形回路では、入力されるディジタル信号は、レベルシフタを介してコンパレータに入力され、所定の参照電圧によって波形整形される。また、レベルシフタから出力されるディジタル信号のハイレベル電圧とローレベル電圧の中間の電圧は、中間電圧検出手段によって検出されて、参照電圧とともに制御手段へ出力される。制御手段は、中間の電圧が参照電圧と等しくなるための制御信号をレベルシフタに出力して、入力されるディジタル信号の直流オフセット電圧を可変する。

【００２４】また、本発明のディジタル信号解析装置では、上記発明の波形整形回路と同一構成の波形整形回路によって波形整形されたコンパレータの出力信号と入力端子から入力されたクロック信号とは、その間の位相が可変遅延器によって可変されて、識別器に入力される。識別器からの判定信号は、誤り測定器によって、入力さ

れたディジタル信号に相当する基準信号と比較される。誤り測定器によって検出された誤り信号は、第２の制御手段に入力される。第２の制御手段は、誤り測定器からの誤り信号を受けながら、可変遅延器の遅延量を可変し、相隣り合って誤り信号が最大となる遅延量のほぼ中間遅延量を検出して、可変遅延器に出力する。

【００２５】

【実施例】以下、図面に基づいて本発明の第１実施例を説明する。

【００２６】図１は、第１の実施例の波形整形回路１０の構成を示す回路図である。

【００２７】図１において、端子１１に入力される入力ディジタル信号は、入力抵抗R_0（例えば５０Ω）で終端され、レベルシフタ１２に入力される。

【００２８】レベルシフタ１２は、入力ディジタル信号の平均直流（オフセット）電圧レベルを、後述する制御回路２１からの誤差信号（制御信号）Ｖｅの大きさに応じて可変する。このために、レベルシフタ１２は、例えば図２に示すように構成されている。

【００２９】即ち、入力ディジタル信号の平均直流電圧は、抵抗R_1とコンデンサC_1による積分回路で検出され、加算器１３に入力される。加算器１３は、誤差信号Ｖｅをこの平均直流電圧に加算し、その加算電圧を、抵抗R_2を介して出力する。抵抗R_2と端子１１との間には、入力ディジタル信号の交流成分のみを通過させるコンデンサC_2が設けられている。したがって、コンデンサC_2と抵抗R_2との接続点からは、入力ディジタル信号の交流成分に加算器１３からの出力電圧が加えられた信号、即ち、入力ディジタル信号に対して誤差電圧Ｖｅだけレベルがシフトされた信号が出力される。

【００３０】なお、抵抗R_1、R_2は、５０Ωの伝送インピーダンスに影響のない数１０ＫΩ程度の高抵抗値を有する。

【００３１】レベルシフタ１２の出力は、図１に示すように、中間電圧検出回路１５および後述するコンパレータ２０へ入力されている。

【００３２】中間電圧検出回路１５は、レベルシフタ１２の出力信号の最大電圧を検出する最大値検出回路１６と、レベルシフタ１２の出力信号の最小電圧を検出する最小値検出回路１７と、両検出回路１６、１７の出力電圧間の中間の電圧を、互いに直列接続された同一抵抗値の２つの抵抗R_3、R_4の接続点から出力する中間電圧出力回路１８によって構成されている。

【００３３】コンパレータ２０は、一方の入力端子ＩＮに入力されるレベルシフタ１２の出力信号のレベルが、他方の入力端子ＲＥＦに加えられる所定の参照電圧（以下しきい値電圧ともいう）Ｖｒより大きいときにハイレベル、小さいときにローレベルのディジタル信号を出力する。このコンパレータ２０は、超高周波用の半導体素子（例えばガリウム－ヒ素型ＦＥＴ）等で構成されている。

【００３４】中間電圧検出回路１５から出力される中間の電圧Ｖｏと、しきい値電圧Ｖｒは、この波形整形回路１０の制御手段である制御回路２１に入力されている。制御回路２１は、入力される中間の電圧Ｖｏとしきい値電圧Ｖｒとの差を減算器２２によって検出し、その差電圧信号を低域通過フィルタ２３を介してレベルシフタ１２に出力して、中間の電圧Ｖｏがしきい値電圧Ｖｒに一致する方向にレベルシフタ１２のシフト量を制御する。

【００３５】図３は、中間電圧検出回路１５および制御回路２１のより具体的な回路の一例を示している。

【００３６】即ち、最大値検出回路１６は、レベルシフタ１２の出力にアノード側を接続されたダイオード１６ａと、ダイオード１６ａのカソードと接地間に接続されたコンデンサ１６ｂとによって形成された正方向のピーク検波回路を有し、このダイオード１６ａとコンデンサ１６ｂとの接続点と所定の負電源$-V_1$との間には、ダイオード１６ａに微少の順方向バイアス電流を流す定電流源１６ｃが接続されている。

【００３７】また、最小値検出回路１７は、レベルシフタ１２の出力にカソード側を接続されたダイオード１７ａと、ダイオード１７ａのアノード側と接地間に接続されたコンデンサ１７ｂとによって形成された負方向のピーク検波回路を有し、ダイオード１７ａとコンデンサ１７ｂとの接続点と所定の正電源$+V_1$との間には、ダイオード１７ａに微少の順方向バイアス電流を流す定電流源１７ｃが接続されている。

【００３８】したがって、最大値検出回路１６のダイオード１６ａとコンデンサ１６ｂとの接続点からは、レベルシフタ１２から出力されるディジタル信号のうち、負電源$-V_1$電圧以上のハイレベル電圧が出力され、最小値検出回路１７のダイオード１７ａとコンデンサ１７ｂとの接続点からは、正電源$+V_1$電圧以下のローレベル電圧が出力されることになる。

【００３９】各ダイオード１６ａ、１７ａに対する定電流源１６ｃ、１７ｃからの順方向バイアス電流は、入力ディジタル信号に対してほとんど影響を与えず、しかも各ダイオード１６ａ、１７ａの検波動作の非直線性を補償するのに必要な１μＡ程度の電流値に設定されている。

【００４０】なお、コンデンサ１６ｃ、１７ｃの容量値は、各ダイオード１６ａ、１７ａに対する順方向バイアス電流が１μＡ程度であることを考慮して、繰返し周期１ＫＨｚ以上のディジタル信号のピーク値をホールドできる１０００ＰＦ程度の値に設定されている。

【００４１】制御回路２１の減算器２２は、差動増幅器２２ａと帰還抵抗２２ｂによって形成され、中間電圧Ｖｏとしきい値電圧Ｖｒとの差に応じた電圧が差動増幅器２２ａから出力される。抵抗２３ａとコンデンサ２３ｂで形成された低域通過フィルタ２３は、差動増幅器２２

ａの出力から雑音成分を除いた誤差信号Ｖｅをレベルシフタ１２へ出力する。

【００４２】したがって、中間の電圧Ｖｏがしきい値電圧Ｖｒに対して低下すると、差動増幅器２２ａの出力電圧は上昇するため、誤差信号Ｖｅが上昇してレベルシフタ１２から出力されるディジタル信号のレベルが全体に上昇する。逆に中間の電圧Ｖｏがしきい値電圧Ｖｒに対して上昇すると、差動増幅器２２ａの出力電圧は低下するため、誤差信号Ｖｅが低下してレベルシフタから出力されるディジタル信号のレベルが全体に低下することになる。

【００４３】次に、上記の波形整形回路１０の動作を説明する。

【００４４】今、仮に、時刻t_0で、レベルシフタ１２に対して入力されるディジタル信号の最大値と最小値の中間値が、図４の（ａ）に示すようにコンパレータ２０のしきい値電圧Ｖｒに等しいとする。

【００４５】この場合、制御回路２１の減算器２２の出力は零となるので、レベルシフタ１２に入力されるディジタル信号は、そのままコンパレータ２０に入力され、しきい値電圧Ｖｒで波形整形される。

【００４６】そして時刻t_1において、図４の（ａ）に示すように、入力されるディジタル信号の直流オフセット電圧がステップ状に上昇したとする。これに応じてレベルシフタ１２の出力信号も同図の（ｂ）に示すように上昇変化し、中間電圧検出回路１５の最大値検出回路１６、最小値検出回路１７の出力電圧も同図の（ｃ）、（ｄ）に示すようにステップ状に変化する。

【００４７】このため、減算器２２への中間の電圧Ｖｏも同図の（ｅ）に示すようにステップ状に変化し、減算器２２の出力は、同図の（ｆ）に示すようにマイナス方向に大きく変化する。

【００４８】したがって、低域通過フィルタ２３からは、同図の（ｇ）に示すように、その時定数に応じた速度で下降する誤差信号Ｖｅが出力される。

【００４９】このため、レベルシフタ１２のシフト量もマイナス側に除々に増加するので、コンパレータ２０に入力されるディジタル信号の中間値は、同図の（ｂ）に示すように、しきい値電圧Ｖｒに一致する方向に変化する。

【００５０】この結果、時刻t_2においては、減算器２２の入力電圧間の差はほぼ零となり、以降は、この安定状態が継続され、確実に波形整形されたディジタル信号がコンパレータ２０の出力から得られる。

【００５１】以後、入力ディジタル信号のオフセットが変化しても、コンパレータへ入力されるディジタル信号の中間の電圧は、しきい値電圧Ｖｒに近づく方向に常にフィードバック制御されるため、確実な波形整形動作が安定して継続する。

【００５２】

【第２の実施例】なお、前記第１の実施例では、レベルシフタ１２のシフト量を制御するための制御ループを常に閉じていたが、入力ディジタル信号に対するシフト量が安定して適正量になった後、このシフト量をホールドしてループを開くとともに、信号ラインに接続されている中間電圧検出回路１５の検波動作を停止させるように構成することもできる。

【００５３】図５は、第２の実施例であるこのホールド型の波形整形回路１０′の構成を示している。この波形整形回路１０′は、ホールド信号（停止信号）を受けて誤差信号の大きさを保持するホールド回路２５と、ホールド信号（停止信号）によって閉じて最大値検出回路１６、最小値検出回路１７のダイオード１６ａ、１７ａに逆バイアス電圧$\pm V_2$を与えるスイッチ２６、２７（停止手段）とを有している。

【００５４】このように構成された波形整形回路１０′では、入力ディジタル信号に対するレベルシフタ１２のシフト量が、前記同様のループ制御によって適正量になった後に、ホールド信号（停止信号）を入力すると、適正なシフト量を与える誤差信号Ｖｅの値がホールド回路２５にホールドされて、レベルシフタ１２のシフト量が適正量に固定される。また、このとき、中間電圧検出回路１５の両検出回路１６、１７のダイオード１６ａ、１７ａは、逆バイアス電圧によってディジタル信号のラインから電気的に切離されるため、このラインに対するダイオード接続の悪影響（高周波特性の悪化）を防ぐことができる。

【００５５】なお、図５に示した波形整形回路１０′では、ホールド信号によって、逆方向バイアス電圧$\pm V_2$を最大値検出回路１６と最小値検出回路１７に単に印加する場合について説明したが、図３に具体例を示した中間電圧検出回路１５のように、ダイオード１６ａ、１７ａに対して定電流源１６ｃ、１７ｃから順方向の微少電流を加えている場合には、この定電流源と逆バイアス電圧$\pm V_2$との切換えを、ホールド信号によって行なうようにしてもよい。

【００５６】図６は、定電流源１６ｃ、１７ｃと逆バイアス電圧$\pm V_2$とを切換えることによって、中間電圧検出回路１５の検波動作を停止させる停止回路２９の具体的な回路構成を示している。

【００５７】この停止回路２９は、前述のホールド信号を停止信号として受けて、スイッチ２６′、２７′をノーマルモードからホールド／リミッタモードへ切換える。ノーマルモードにおいて、ダイオード１６ａ、１７ａには、前記同様に微少な順方向バイアス電流が定電流源１６ｃ、１７ｃから供給されるため、中間電圧検出回路１５は、レベルシフタ１２からのディジタル信号の最大値、最小値の検出を行なう。

【００５８】ホールドモードにおいては、入力ディジタル信号の最大、最小値よりも十分に大きい（例えば、４

ボルト程度）逆バイアス電圧±V_2 が、ダイオード１６ａ、１７ａに加えられるため、中間電圧検出回路１５は、最大値、最小値の検出動作を停止する。

【００５９】リミッタモードにおいては、ダイオード１６ａ、１７ａの順方向電圧降下分０．７ボルトを見込んだ１．３ボルト程度の逆バイアス電圧±V_2がダイオード１６ａ、１７ａに加えられるため、入力ディジタル信号に対してほぼ±２Ｖでリミッタをかけることができる。

【００６０】以上のように、図６の回路では、逆バイアス電圧±V_2 として設定する電圧を、そのときの状態に応じて４ボルトまたは１．３ボルトになるように可変制御することにより、ホールドモードまたはリミッタモードの両方を上述のノーマルモードと共に切換えて使用することができる。なお、図６において、符号１６ｄ、１７ｄはそれぞれバッファアンプである。

【００６１】また、停止回路２９を図７に示すように構成すれば、前述のノーマルモードおよびホールドモードのいずれの場合でもダイオード１６ａ、１７ａをリミッタ動作させることが可能となる。

【００６２】図７に示した停止回路２９では、ダイオード１６ａ、１７ａに対して常に０．６ボルト程度の逆バイアス電圧±V_3 がダイオード３０、３１を介して印加されている。また、最大値検出回路１６側のスイッチ２６′のホールド側には、最小値検出回路１７側の定電流源１７ｃが接続され、最小値検出回路１７側のスイッチ２７′のホールド側には、最大値検出回路１６側の定電流源１６ｃが接続されている。

【００６３】このため、ノーマルモード時において、ダイオード１６ａ、１７ａにそれぞれの定電流源１６ｃ、１７ｃからの順方向バイアスがかけられて、入力ディジタル信号に対する最大値、最小値検出が行なわれることは前記図６の回路の場合と同様である。

【００６４】しかるに、このノーマルモードにおいて、レベルシフタ１２からの出力電圧が－２Ｖよりも低くなると、最小値検出回路１７のダイオード１７ａおよびダイオード３１が導通するため最小値検出回路１７側は－２Ｖ（－V_3－１．４Ｖ）でリミッタがかかることになる。

【００６５】また、ノーマルモードにおいて、レベルシフタ１２からの出力電圧が＋２Ｖよりも高くなると、最大値検出回路１６側のダイオード１６ａおよびダイオード３０が導通するため、最大値検出回路１６側は＋２Ｖ（＋V_3 ＋１．４Ｖ）でリミッタがかかることになる。

【００６６】なお、以上において、－１．４Ｖはダイオード１７ａ、３１での電圧降下分であり、＋１．４Ｖはダイオード１６ａ、３０での電圧降下分である。

【００６７】また、ホールドモード時において、ダイオード１６ａ、１７ａは、それぞれ定電流源１７ｃ、１６ｃ側からの逆バイアスによって、入力ディジタル信号に対する最大値、最小値検出動作が停止される。

【００６８】しかるに、このホールドモードにおいて、±V_1 ＝±１．３Ｖ程度に設定しておけば、レベルシフタ１２からの出力電圧が－２Ｖよりも低くなるかあるいは＋２Ｖよりも高くなると、それぞれ上述したノーマルモード時と同様に－２Ｖまたは＋２Ｖでリミッタがかかるようになる。

【００６９】なお、前記した図５、図６、図７のホールド回路２５としては、アナログ型のホールド回路の他に図８に示すように、ディジタル型のホールド回路を用いることもできる。

【００７０】図８に示したホールド回路２５は、制御回路２１からの誤差信号ＶｅをＡ／Ｄ変換器３２でディジタル値に変換し、ホールド信号（切換信号）が入力されたときのディジタル値をメモリ回路３３に記憶する。メモリ回路３３に記憶されたディジタル値は、Ｄ／Ａ変換器３４によってアナログ電圧に変換され、スイッチ３５を介してレベルシフタ１２へ出力される。

【００７１】スイッチ回路３５は、ホールド信号が入力されていないとき、制御回路２１からの誤差信号をそのままレベルシフタ１２へ出力し、ホールド信号が入力されているとき、Ｄ／Ａ変換器３４からの信号を出力する。このようなディジタル型のホールド回路は、アナログ型のホールド回路に比べて、ホールド出力の変動が無いため、長時間のホールド動作が必要なときに有利である。

【００７２】また、前記説明では制御回路２１の具体的な回路として、減算器２２と低域通過フィルタ２３とを別構成にしていたが、図９に示すように、演算増幅器２１ａの出力をコンデンサ２１ｂによって帰還する積分型の回路を用いて制御回路を簡単化することもできる。

【００７３】また、前記実施例において、レベルシフタ１２におけるシフト量を知りたい場合には、誤差信号Ｖｅの大きさを電圧計で読んだり、図１０に示すように、抵抗R_5 とコンデンサC_5 の積分回路でそれぞれ検出されたレベルシフタ１２の入出力間の平均直流電圧の差を、電圧計３７で読むようにすれば、レベルシフタ１２のシフト量を知ることができる。また、このレベルシフト量から入力ディジタル信号のスレッショルドレベルを知ることができる。なお、図８に示したディジタル型のホールド回路２５を用いた場合、Ａ／Ｄ変換器３２によってレベルシフタ１２におけるシフト量を検知することができるので、図１０のような回路は不要である。

【００７４】また、前記実施例は、超高周波で使用される波形整形回路について説明したが、本発明の波形整形回路は、低い周波数帯の波形整形回路にも適用することができる。

【００７５】さらに、コンパレータとしては、前記実施例のガリウム－ヒ素型のＦＥＴで構成されたものだけでなく、例えば、シリコンバイポーラトランジスタやヘテ

ロバイポーラトランジスタ（ＨＢＴ）で構成されたコンパレータを用いてもよい。また、レベルシフタについても前記実施例の構成の他に、直流阻止コンデンサと高周波阻止コイルで構成されたレベルシフタ等種々のものが使用できる。

【００７６】

【第３の実施例】次に、以上のような波形整形回路を用いるディジタル信号解析装置について説明する。

【００７７】図１１は、第３の実施例として、本発明のディジタル信号解析装置を誤り測定装置に適用した場合の構成を示すブロック図である。

【００７８】この誤り測定装置は、クロック信号とともに入力される被測定データ信号を波形整形した後、その２値判定を、入力されたクロック信号に同期したタイミングで識別し、識別された信号を入力されたディジタル信号に相当する基準信号のデータと比較するように構成されている。

【００７９】被測定データ信号は、前述した図１の波形整形回路１０と同一構成の波形整形回路５０に入力される。

【００８０】即ち、入力端子５１から入力された被測定データ信号は、入力抵抗R_0（例えば５０Ω）で終端され、レベルシフタ５２に入力される。レベルシフタ５２は、入力された被測定データ信号の直流平均（オフセット）電圧を、誤差信号Ｖｅの大きさに応じて可変する。

【００８１】レベルシフタ５２の出力は、中間電圧検出回路５５およびコンパレータ６０に入力される。中間電圧検出回路５５は、レベルシフタ５２から出力されるディジタル信号のハイレベルのピーク電圧とローレベルのピーク電圧を、ハイレベルピーク検出回路（最大値検出回路）５６とローレベルピーク検出回路（最小値検出回路）５７でそれぞれ検出し、その中間の電圧Ｖｏを、等しい２つの抵抗Ｒの中点から出力する。

【００８２】この中間の電圧Ｖｏは、参照電圧発生器５９からの参照電圧（しきい値電圧）Ｖｒとともに第１の制御回路６１に入力される。

【００８３】第１の制御手段である第１の制御回路６１は、参照電圧Ｖｒと中間の電圧Ｖｏとの差を検出する減算回路６２と、減算回路６２の減算出力を積分して得た誤差信号Ｖｅを出力する低域通過フィルタ（以下、ＬＰＦと記す）６３で構成され、中間の電圧Ｖｏが常に参照電圧Ｖｒに近づく方向にレベルシフタ５２のシフト量をフィードバック制御する。

【００８４】コンパレータ６０は、レベルシフタ５２から出力されるディジタル信号が、参照電圧Ｖｒより高いときハイレベル、低いときローレベルのディジタル信号を出力して、入力されたディジタル信号を波形整形する。

【００８５】以上の構成は、前述したように、図１に示した波形整形回路１０と全く同一であり、各部の詳細および変形例については、前述の説明によるものとする。

【００８６】一方、入力端子７０に入力されたクロック信号は可変遅延器７１を介して、識別器７２および誤り測定器である誤り測定部７５へ入力されている。可変遅延器７１は、入力されるクロック信号を制御信号に応じて遅延し、被測定データ信号に対するクロック信号の位相を相対的に可変する。この可変遅延器７１としては、信号線路長をスラグ可変することによって、その遅延量を可変する可変長スラブライン構造のものが、超高周波用として用いられる。

【００８７】識別器７２は、コンパレータ６０から出力されるディジタル信号のレベルを、可変遅延器７１から入力されるクロック信号の立上り（または立下がり）のタイミングで２値判定し、その識別出力を、誤り測定部７５へ出力する。

【００８８】この実施例による誤り測定装置のデータ解析部である誤り測定部７５は、基準データ発生器７６、符号比較器７７、不一致カウンタ７８およびクロックカウンタ７９によって構成されている。

【００８９】基準データ発生器７６は、測定しようとするデータと同一パターンの基準データを、可変遅延器７１からのクロック信号に同期したタイミングで符号比較器７７へ出力する。

【００９０】符号比較器７７は、識別器７２の出力と基準データとの符号の一致、不一致を判定し、不一致の場合には、不一致信号を不一致カウンタ７８へ出力する。

【００９１】不一致カウンタ７８は、後述する制御部８０からのゲート信号を受けている間、不一致信号の計数を継続して行なう。クロックカウンタ７９は、制御部８０からのゲート信号を受けている間、可変遅延器７１から出力されるクロック信号の計数を行なう。

【００９２】この誤り測定装置の第２の制御手段である制御部８０は、マイクロプロセッサ（ＣＰＵ）等で構成され、主に２つの処理モードを有している。

【００９３】即ち、第１の処理モードは、不一致カウンタ７８とクロックカウンタ７９を同時に所定時間計数させた後、両カウンタの計数結果を読込んで、符号誤り率の演算を行ない、その結果を表示器８１に表示させる通常の測定処理である。第２の処理モードは、測定処理の前に、可変遅延器７１のクロック信号に対する遅延量を所定範囲連続的に可変して、その遅延量に対する誤り率データを求め、メモリ８０ａに記憶して、誤り率が最小となる遅延量を検出する最適遅延量検出処理である。

【００９４】なお、図１１中のＡ／Ｄ変換器６５は、波形整形回路５０の第１の制御回路６１からの誤差信号Ｖｅをディジタル値に変換し、この値をレベルシフタ５２のシフト量として制御部８０へ出力する。制御部８０は、このシフト量をメモリ８０ａに記憶したり、表示器８１に表示させる。

【００９５】次に、この誤り測定装置の動作について説

明する。

【００９６】入力端子５１、７０に、それぞれ被測定データ信号とクロック信号が入力されると、波形整形回路５０は、入力された被測定データ信号のハイレベルとローレベルの中間の電圧Ｖｏを参照電圧Ｖｒに一致させる方向に、シフト量を制御する。

【００９７】この動作は、前述の図４によって説明した動作と全く同一である。

【００９８】このため、コンパレータ６０からは、図１２の（ａ）に示すように、しきい値電圧（参照電圧）Ｖｒで波形整形され、振幅方向にゆらぎのない被測定データ信号が出力される。

【００９９】なお、レベルシフタ５２のシフト量が安定したことは、Ａ／Ｄ変換器６５からのシフト量を表示器８１に表示させるか、あるいは、制御部８０自身でその安定判定処理を行なうことによって確認することができる。

【０１００】次に、制御部８０は前述した最適遅延量検出処理を行なう。

【０１０１】即ち、制御部８０は、ゲート信号を所定時間クロックカウンタ７９へ入力した後、その計数結果からクロック信号の周期Ｔを求める。そして、図１２の（b_1）、（b_2）、（b_3）に示すように、可変遅延器７１の遅延量を、初期値D_0から所定ステップｄで少なくともクロック信号の１周期分まで可変しながら、所定ステップ毎に誤り率を求め、その結果をメモリ８０ａに記憶する。

【０１０２】図１２の（ｃ）は、メモリ８０ａに記憶された遅延量の変化に対する誤り率の変化を示している。この図から明らかなように、位相成分にゆらぎのあるコンパレータ６０の出力信号（同図の（ａ））に対し、同図の（b_1）から同図の（b_3）までクロック信号の立上りタイミングを１．５周期分可変したときの誤り率の変化は、コンパレータ６０の出力信号の状態遷移点で最大となり、その最大点が２箇所得られる。

【０１０３】制御部８０は、記憶した誤り率のデータに基づいて、例えば誤り率が最大となる遅延量D_2、D_6の中間値D_4を、最も位相余裕のある最適な遅延量として可変遅延器７１に自動設定する。

【０１０４】以上の設定を行なった後、制御部８０は、通常の誤り測定処理を行なって、測定された誤り率を順次表示器８１に表示させる。

【０１０５】なお、Ａ／Ｄ変換器６５からのレベルシフト量や、このレベルシフト量とコンパレータ６０への参照電圧Ｖｒから算出される被測定データ信号のスレッショルドレベルも表示器８１に随時表示される。

【０１０６】また、この第３の実施例の誤り測定装置では、中間の電圧と参照電圧との減算結果をＬＰＦ６３を介して、レベルシフタ５２に入力していたが、図１３に示すように、減算結果をＡ／Ｄ変換器６５で減算データにディジタル変換し、この減算データが零に近づくためのシフト量を、演算制御部９０によって算出し、この算出されたシフト量データをＤ／Ａ変換器６６に送出して、レベルシフタ５２のシフト量を制御するように構成してもよい。なお、この演算制御部９０は、制御部８０とともに、１つのＣＰＵに構成されている。

【０１０７】さらに、中間電圧検出回路５５から出力される中間の電圧を直接Ａ／Ｄ変換して、演算制御部９０へ送り、演算制御部９０によってこの中間電圧データを参照電圧データと比較して、その差に応じたシフト量データをＤ／Ａ変換器６５を介してレベルシフタ５２に出力するように構成することも可能である。この場合には、演算制御部９０が第１の制御手段となる。

【０１０８】また、前記第３の実施例では、クロック信号に対する最適な遅延量を設定するために、クロック信号の１周期分以上にわたって遅延量を可変して得られた誤り率の最大値から、最適値を決定していたが、誤り率が最小値となる遅延量をそのまま最適値として設定するようにしてもよい。これは、入力出信号の位相のゆらぎが大きく、図１２の（ｃ）のD_3からD_5の間の平坦部が極めて狭い場合に有効な方法である。

【０１０９】また、前記実施例のように最大の誤り率でなく、等しい誤り率を与える２つの遅延量（例えば図１２のD_3、D_5）の中間値を最適な遅延量として設定するようにしてもよい。

【０１１０】また、表示器に設けたスイッチ等の入力手段を操作することによって、被測定データ信号の最適スレッショルド電圧を設定する一連の動作を開始し、その動作が終了した後、最適な遅延量を設定する動作を行ない、設定されたスレッショルドレベルと遅延量とを表示器に表示するようにしてもよい。

【０１１１】また、前記第３の実施例では、クロック信号側の位相を遅延させていたが、これは本発明を限定するものでなく、例えば図１４に示すように、可変遅延器７１を、被測定データ信号側の入力端子５１とレベルシフタ５２の間に設けてもよい。また、可変遅延器７１をレベルシフタ５２とコンパレータ６０の間、あるいは、コンパレータ６０と識別器７２の間に設けてもよい。

【０１１２】また、前記第３の実施例では、図１に示した波形整形回路１０と同一構成の波形整形回路５０によって、入力信号の波形整形を行なっていたが、シフト量のホールド機能と中間電圧検出回路５５の動作停止機能を有する第２の実施例（図５）の波形整形回路１０′を用いてもよい。また、同様に図５の変形例としての前述の図６、図７に示したリミッタ機能を有する回路を用いてもよい。

【０１１３】また、前述した図１３の回路をさらに図１５のように変形して、前述の図８で説明したディジタル型のホールド回路を形成してもよい。

【０１１４】この構成の、演算制御部９０は、波形整形

回路５０のループが安定して最適なシフト量になったことを自ら判定して、ホールド信号（停止信号）をスイッチ回路３５および停止回路６９へ出力し、最適なシフト量をレベルシフタ５２へ固定設定するとともに、中間電圧検出回路５５の検出動作を停止させる（なお、停止回路６９は、前述の停止回路２９と同様の構成からなる）。

【０１１５】なお、このように、レベルシフタ５２への最適シフト量の設定制御および中間電圧検出動作の停止制御を行なう演算制御部９０と、可変遅延器７１に対する最適遅延量の設定制御を行なう制御部８０とを、１つのＣＰＵで構成しておけば、簡単なキー操作等によって、被測定データ信号に対する最適シフト量の設定処理と最適遅延量の設定処理とを一連のプログラムによって連続して行なわせることができ、しかも、他装置とのデータの授受をＣＰＵの通信機能を用いて簡単に行なうことができるという利点がある。

【０１１６】図１６は本発明の第３の実施例の誤り測定装置のより具体的な例を示し、特に、超高周波の被測定データ信号の誤り測定を行なう装置の例である。

【０１１７】図１６において、波形整形回路１０１に加えられる入力データおよび可変遅延器１０２に加えられる入力クロックは、それぞれ上述したように適正化されて識別器１０３に出力される。

【０１１８】この識別器１０３で上述したような識別がなされたデータは、１／Ｎデマルチプレクサ１０４において、可変遅延器１０２の出力クロックに基づいてタイミング発生部１０５から発生する１／Ｎクロックによって、１／Ｎにデマルチプレクスされる。例えば、入力データが１０ＧＨｚでＮ＝３２の場合、入力データは、３１０ＭＨｚにデマルチプレクスされて３２チャンネルデータとしてエラー検出部１０６でエラー検出される。このエラー結果は、エラー計数部１０７を介して表示部１０８および同期制御部１０９に送られる。基準パターン発生部１１０は、この同期制御部１０９からの出力に従ってエラー検出部１０６に与えるための基準パターンデータを発生する。

【０１１９】このエラー検出部１０６、基準パターン発生部１１０およびエラー計数部１０７、同期制御部１０９は、タイミング発生部１０５からの１／Ｎクロックにより制御される。ＣＰＵで構成される制御部１１１は各部を制御する。なお、オートサーチ部１１２は、制御部１１１の制御の下に波形整形回路１０１および可変遅延器１０２を前記各実施例と同様にそれぞれ適正な状態に制御する。

【０１２０】この誤り測定装置では、前記実施例と同様に識別器１０３で最適のタイミングで識別されたデータ信号が、１／Ｎの速度の並列データに分割されてエラー判定されるため、超高周波のデータ信号の誤り測定を確実に行なうことができる。

【０１２１】なお、上記実施例は、本発明のディジタル信号解析装置を誤り測定装置に適用した例について説明したが、ロジックアナライザ等の他のディジタル解析装置にも同様に適用できる。

【０１２２】

【発明の効果】以上説明したように、本発明の波形整形回路は、入力ディジタル信号の直流オフセット電圧すなわち、レベルシフタの出力信号のハイレベル電圧とローレベル電圧との中間の電圧を、所定のしきい値に近づける方向にレベルシフタのシフト量を制御し、そのレベルシフタの出力信号を所定のしきい値で波形整形するように構成されている。

【０１２３】このため、煩しい波形観測や手動調整をすることなしに、コンパレータに入力されるディジタル信号の振幅の中心が、常に所定のしきい値に一致した状態に追込まれ、確実な波形整形を行なうことができる。

【０１２４】また、レベルシフタに対する誤差信号の大きさを保持する保持回路と、中間電圧検出回路の動作を停止させる停止手段を設けた波形整形回路では、シフト量を適正量に固定することができ、信号路の高周波特性を悪化させずに済むという効果がある。

【０１２５】また、本発明のディジタル信号解析装置は、前記説明のように、前記波形整形回路から出力されるディジタル信号とクロック信号との位相を相対的に所定範囲遅延可変して得られた誤り測定結果に基づいて、コンパレータから識別器へ入力されるディジタル信号の隣り合う状態遷移点の間の最適位置に、識別のタイミングが入るための遅延量を検出し、その遅延量を、可変遅延器に設定するように構成されている。

【０１２６】このため、波形観測をしながらの煩雑な手動による電圧調整や位相調整操作をせずに、コンパレータによる波形整形の動作点や識別タイミングを、波形の乱れによる誤差や個人差のない状態で、最適状態に設定することができる。

【図面の簡単な説明】

【図１】本発明の第１の実施例構成を示すブロック図である。

【図２】図１の要部の具体的な回路の一例を示す回路図である。

【図３】図１の要部の具体的な回路の一例を示す回路図である。

【図４】一実施例の動作を説明するための信号図である。

【図５】本発明の第２の実施例の構成を示すブロック図である。

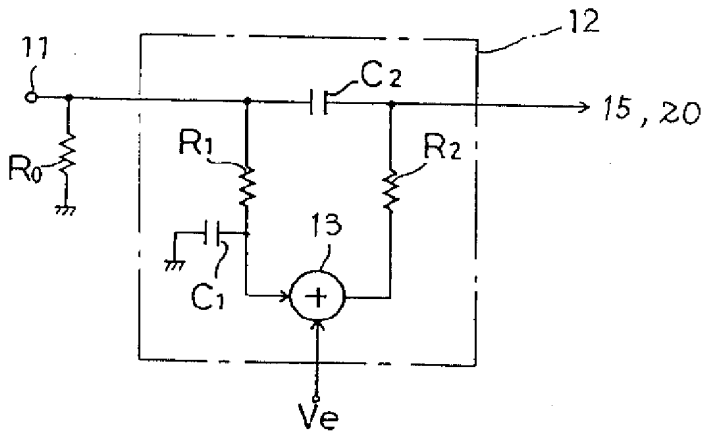
【図６】第２の実施例の要部の変形例を示す回路図である。

【図７】第２の実施例の要部の変形例を示す回路図である。

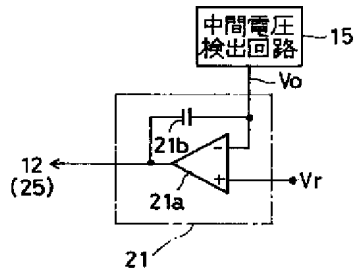
【図８】第２の実施例の要部の変形例を示す回路図であ

る。
【図９】第１、第２の実施例の要部の変形例を示す回路図である。
【図１０】シフト量を直接読みとるための回路図である。
【図１１】本発明の第３の実施例の構成を示すブロック図である。
【図１２】第３の実施例の動作を説明するための図である。
【図１３】第３の実施例の変形例を示す要部ブロック図である。
【図１４】第３の実施例の他の変形例を示すブロック図である。
【図１５】第３の実施例の他の変形例を示すブロック図である。
【図１６】第３の実施例の要部をより具体的に示したブロック図である。
【図１７】従来装置の構成を示すブロック図である。
【図１８】従来装置の動作を説明するための信号図である。
【符号の説明】
１０、１０′　波形整形回路
１２　レベルシフタ
１５　中間電圧検出回路
１６　最大値検出回路
１７　最小値検出回路
１８　中間電圧出力回路
２０　コンパレータ
２１　制御回路
２２　減算器
２３　低域通過フィルタ
２５　ホールド回路
２６、２７　スイッチ
２９　停止回路
３２　Ａ／Ｄ変換器
３３　メモリ回路
３４　Ｄ／Ａ変換器
３５　スイッチ
３７　電圧計
５０　波形整形回路
５２　レベルシフタ
５５　中間電圧検出回路
６０　コンパレータ
６１　第１の制御回路
６５　Ａ／Ｄ変換器
７１　可変遅延器
７２　識別器
７５　誤り測定部
７６　基準データ発生器
７７　符号比較器
７８　不一致カウンタ
７９　クロックカウンタ
８０　制御部
８１　表示器
９０　演算制御部
１０１　波形整形回路
１０２　可変遅延器
１０３　識別器
１０４　１／Ｎデマルチプレクサ
１０５　タイミング発生部
１０６　エラー検出部
１０７　エラー計数部
１０８　表示部
１０９　同期制御部
１１０　基準パターン発生部
１１１　ＣＰＵ
１１２　オートサーチ部

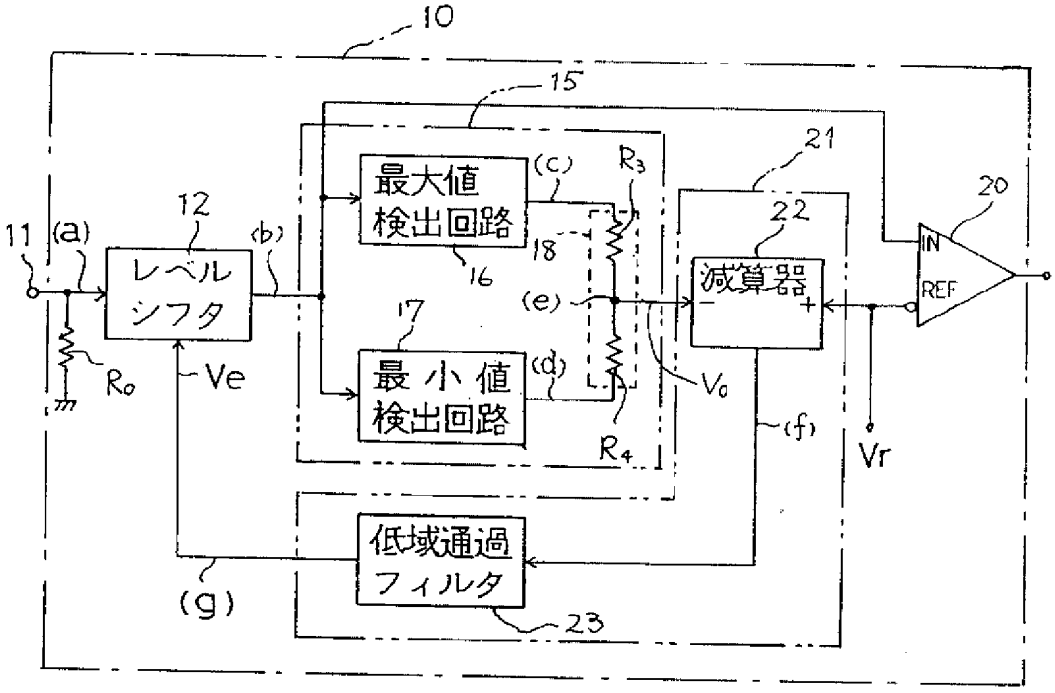
【図２】



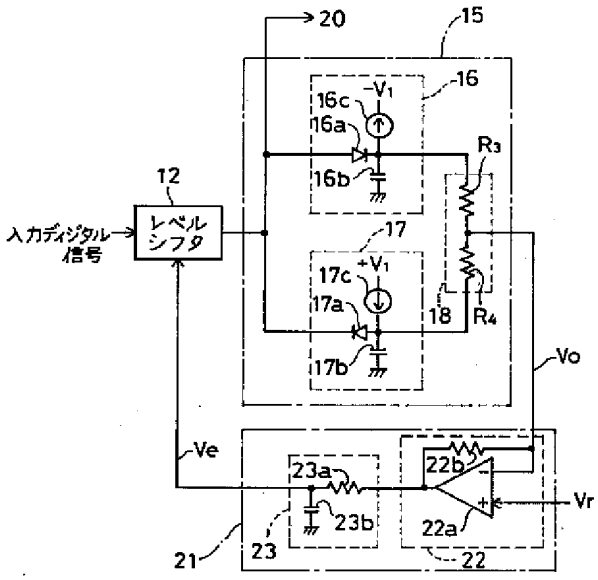
【図９】



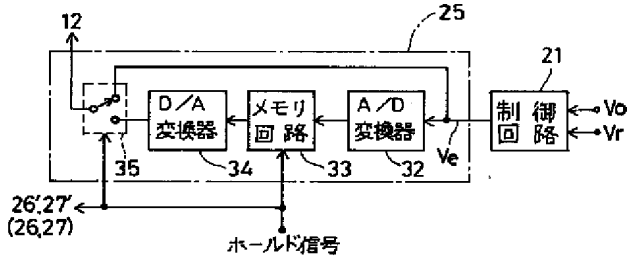
【図１】


10
15
21
20
12
11
(a)
(b)
レベル
シフタ
最大値
検出回路
(c)
R3
18
16
22
減算器
IN
REF
17
最小値
検出回路
(d)
(e)
Ro
Ve
Vo
(f)
R4
Vr
低域通過
フィルタ
(g)
23

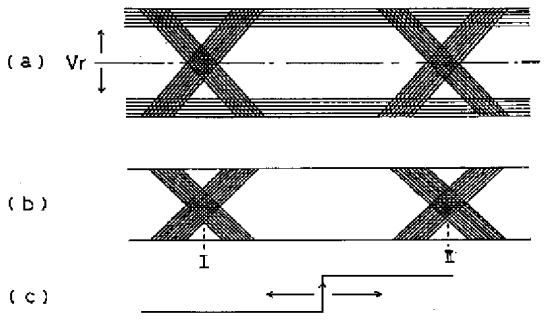
【図３】


20
15
16
16c
-V1
16a
16b
R3
12
入力ディジタル
信号
レベル
シフタ
17
17c
+V1
17a
17b
18
R4
Vo
Ve
23a
22b
Vr
23b
22a
21
23
22

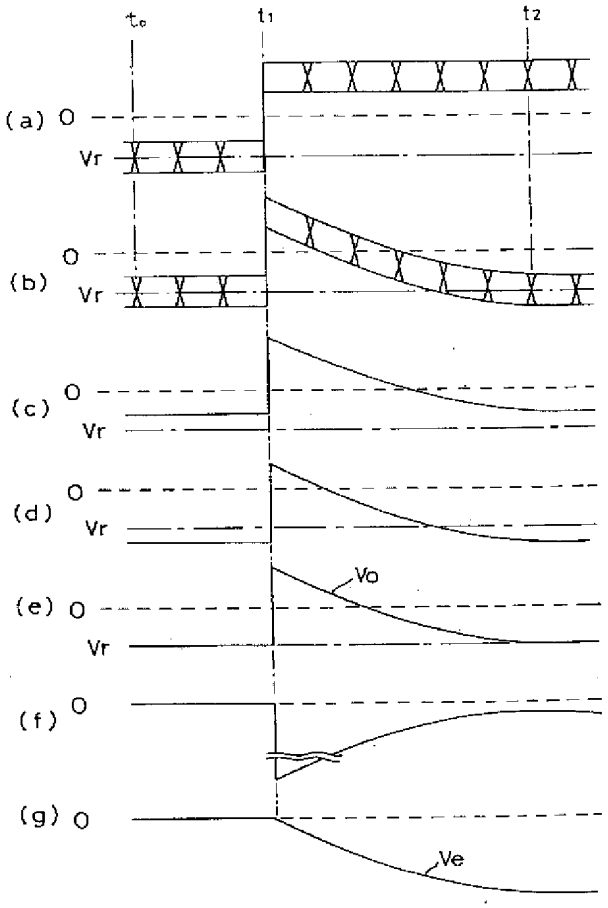
【図８】


12
25
21
D/A
変換器
メモリ
回路
A/D
変換器
制御
回路
Vo
Vr
Ve
35
34
33
32
26'27'
(26,27)
ホールド信号

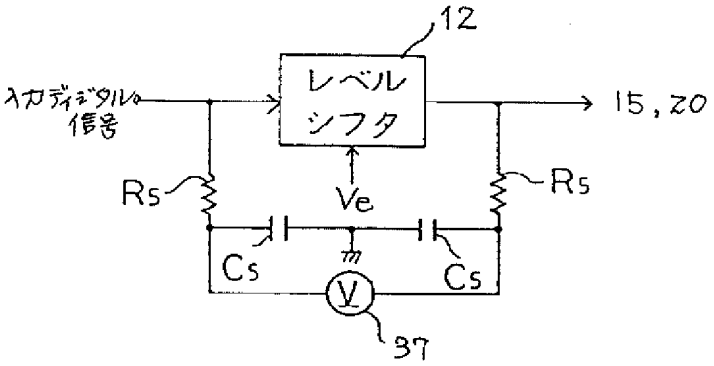
【図１８】


(a)
Vr
(b)
I
I
(c)

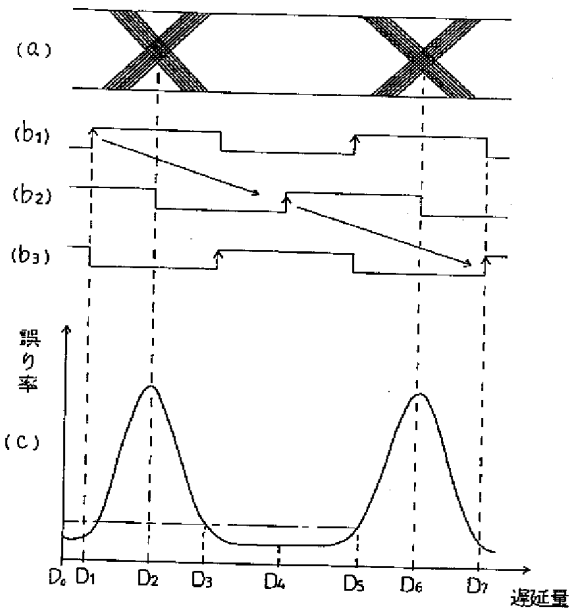
【図４】


t₀
t₁
t₂
(a)
(b)
(c)
(d)
(e)
(f)
(g)
O
Vr
Vo
Ve

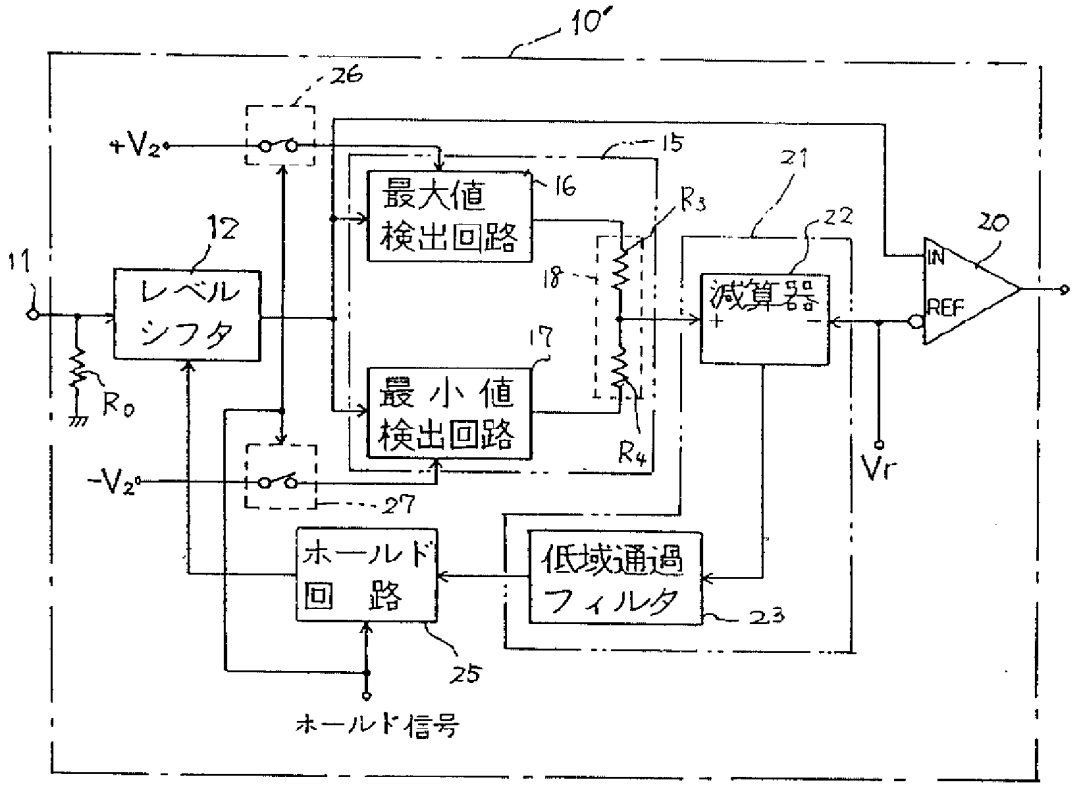
【図１０】


12
レベル
シフタ
入力ディジタル
信号
15, 20
R5
R5
Ve
Cs
Cs
V
37

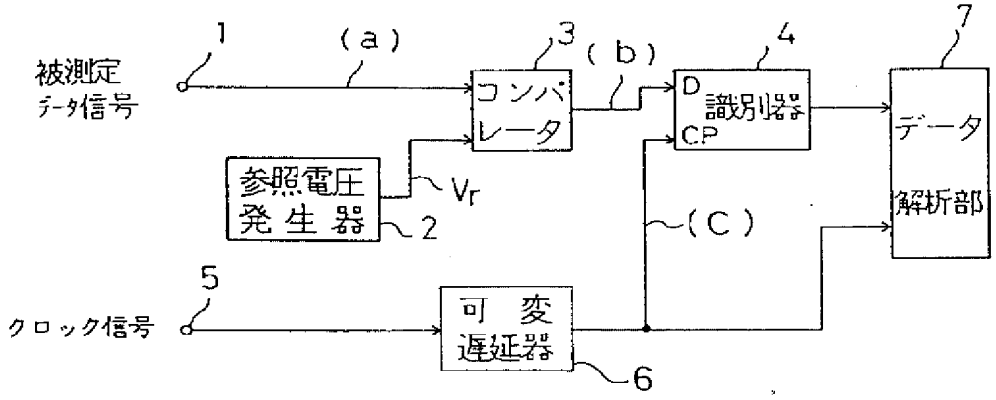
【図１２】


(a)
(b1)
(b2)
(b3)
(c)
誤り率
D0 D1 D2 D3 D4 D5 D6 D7
遅延量

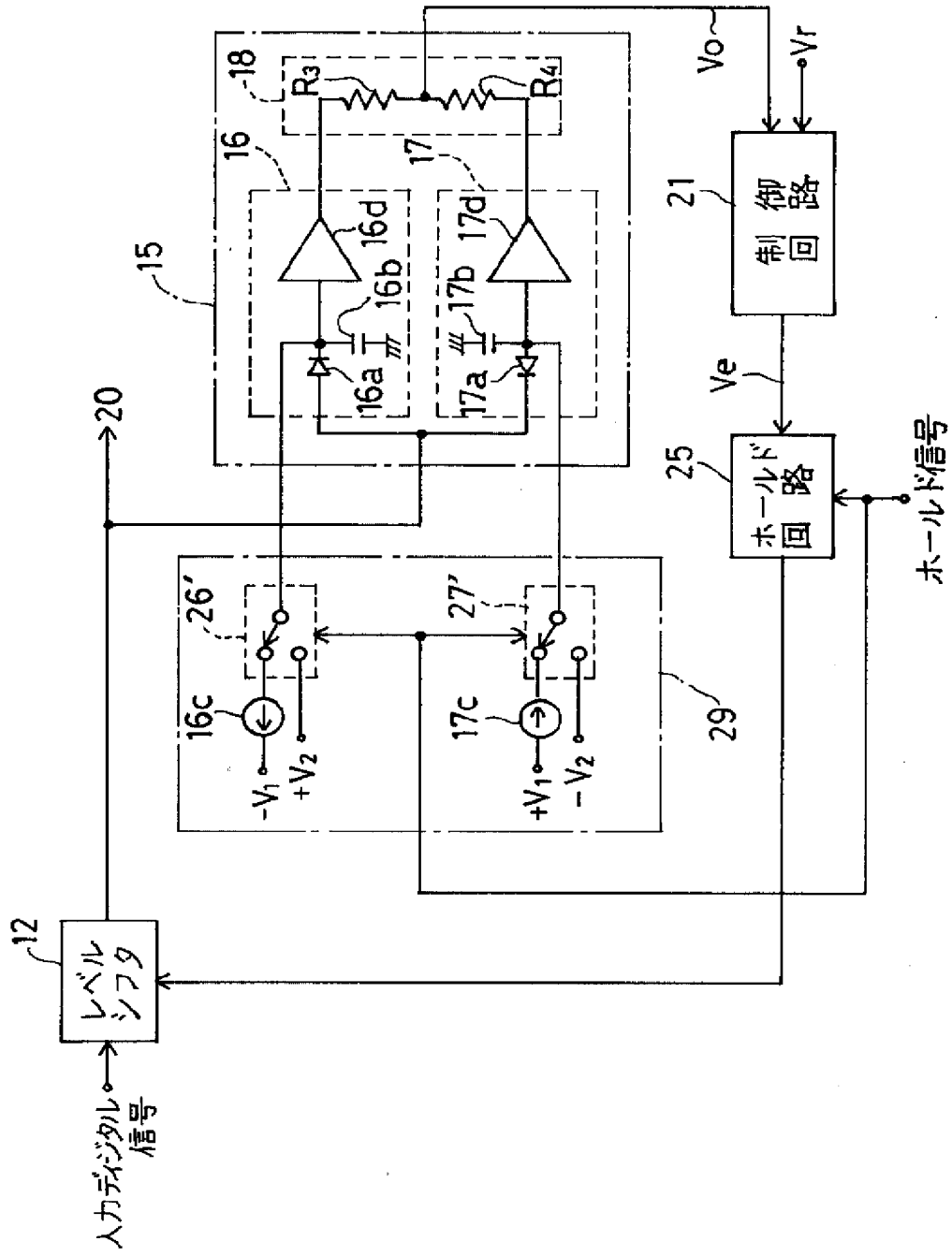
【図５】


10'
26
+V2
15
最大値
検出回路
16
R3
21
22
20
IN
REF
減算器
12
11
レベル
シフタ
18
17
R0
最小値
検出回路
R4
Vr
-V2
27
ホールド
回路
低域通過
フィルタ
23
25
ホールド信号

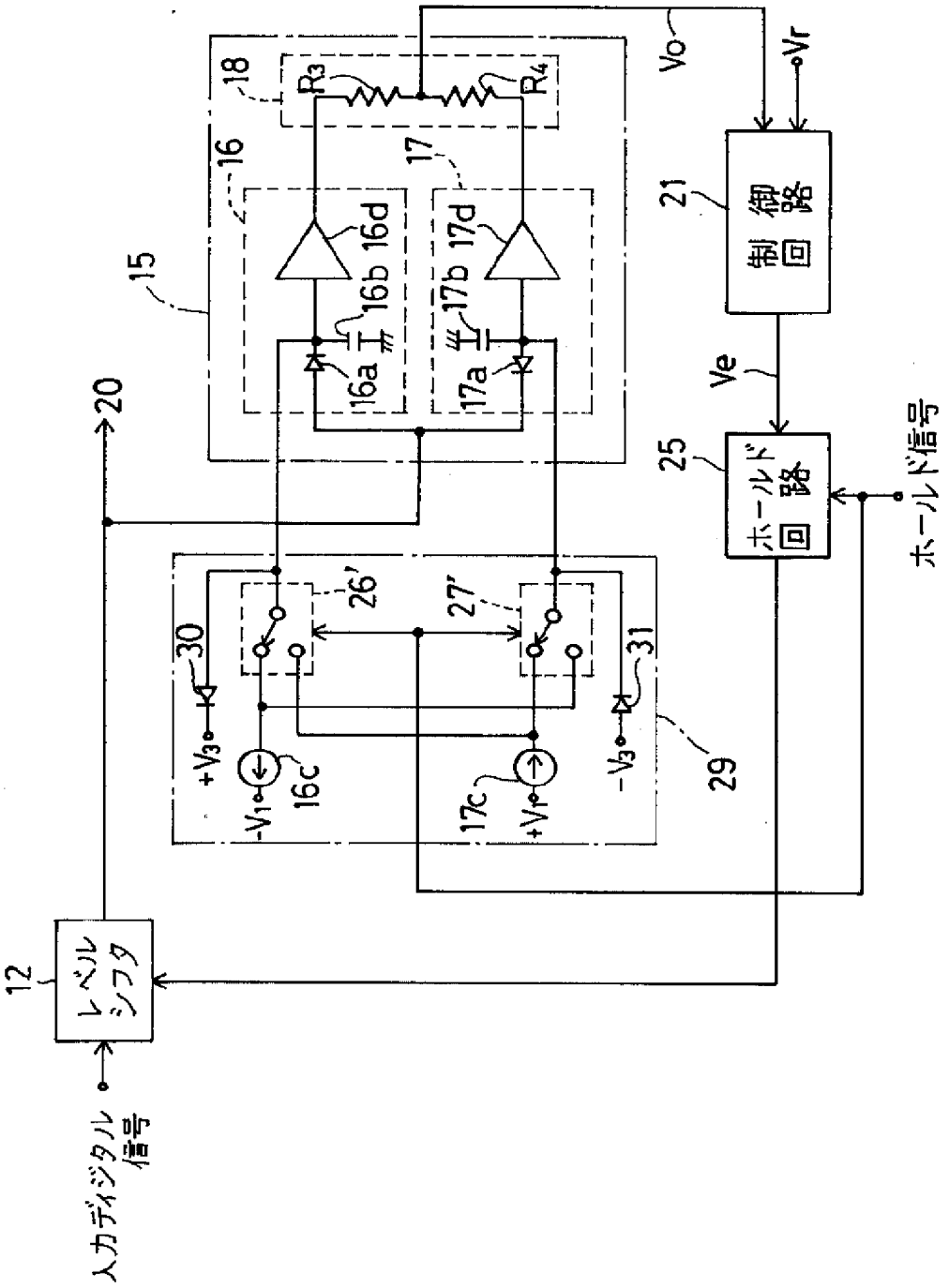
【図１７】


被測定
データ信号
1
(a)
3
コンパ
レータ
(b)
4
D
識別器
CP
7
データ
解析部
参照電圧
発生器
2
Vr
(C)
5
クロック信号
可変
遅延器
6

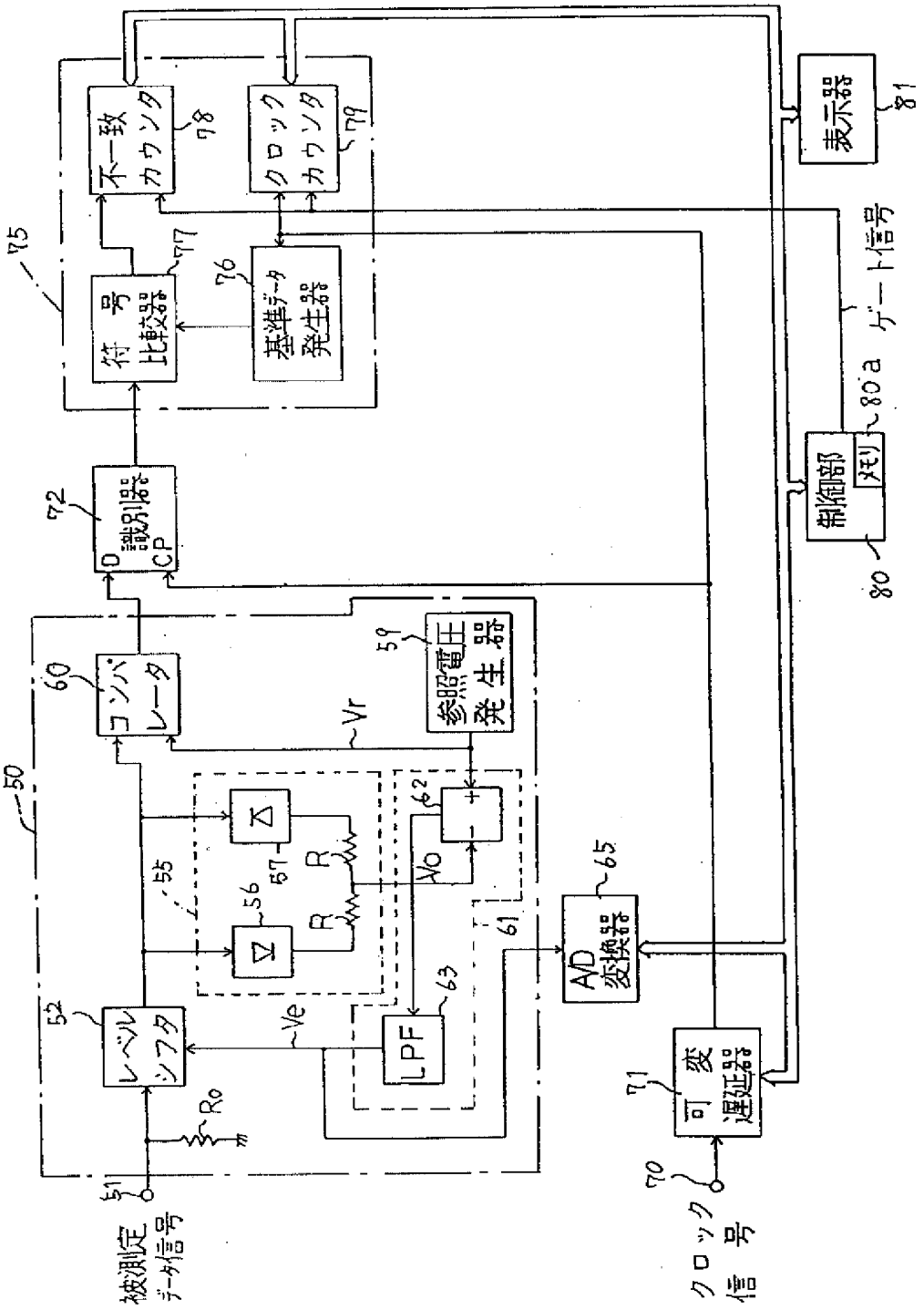
【図6】


Vo
Vr
18
R3
R4
16
17
16d
17d
15
16b
17b
16a
17a
21
制御回路
Ve
20
25
ホールド回路
ホールド信号
26'
27'
16c
17c
-V1
+V2
+V1
-V2
29
12
レベルシフタ
入力ディジタル信号

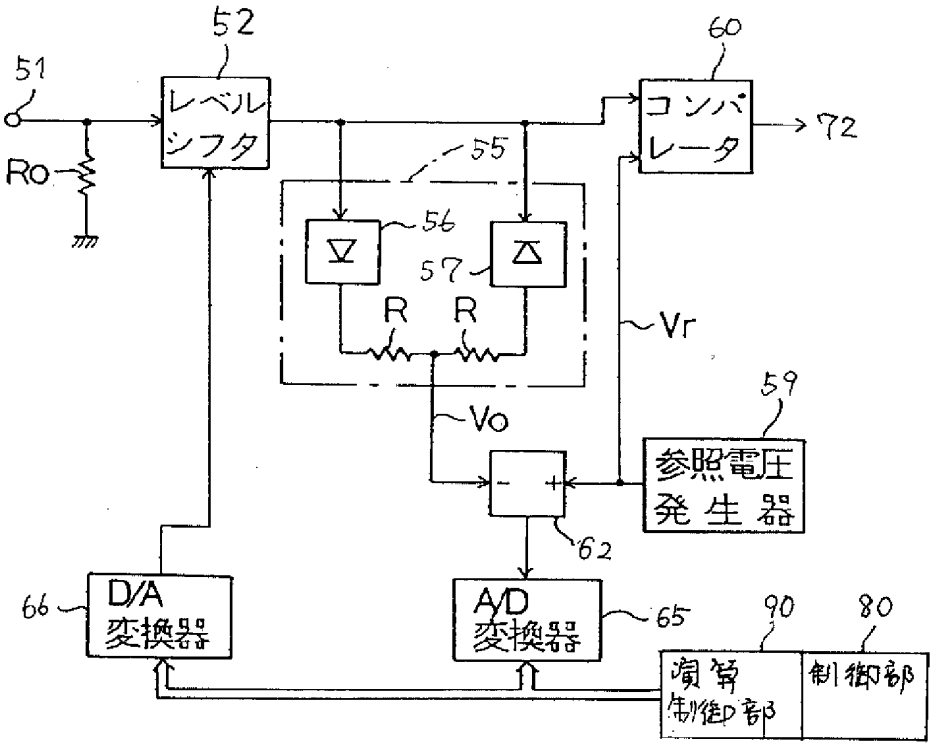
【図7】


入力ディジタル信号
12
レベルシフタ
20
15
16
17
18
R3
R4
16d
17d
16b
17b
16a
17a
21
制御回路
Vo
Vr
Ve
25
ホールド回路
ホールド信号
26'
27'
30
31
+V3
-V3
-V1
+V1
16c
17c
29

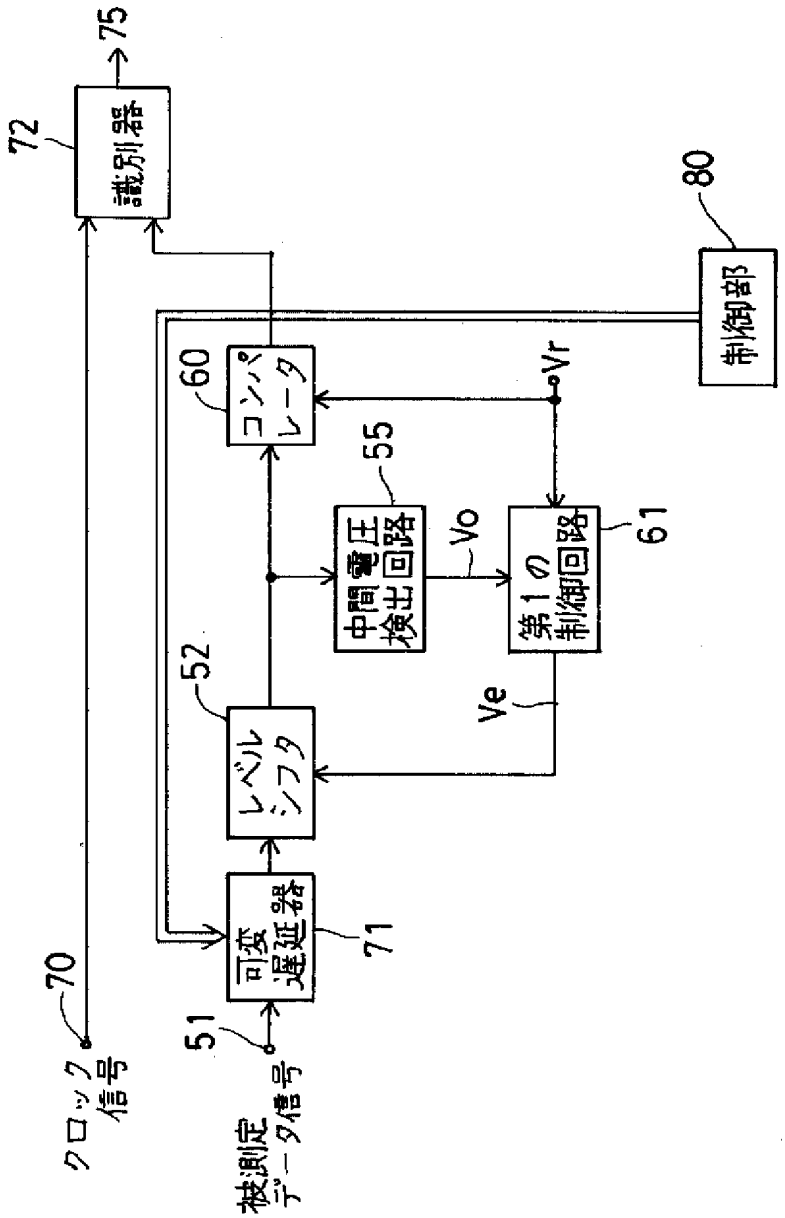
【図11】


不一致カウンタ
78
クロックカウンタ
79
表示器
81
75
符号比較器
77
基準データ発生器
76
ゲート信号
80a
メモリ
制御部
80
識別器
D
CP
72
コンパレータ
60
参照電圧発生器
59
Vr
50
Σ
57
R
56
R
55
Vo
62
+
−
61
A/D変換器
65
レベルシフタ
52
Ve
LPF
63
Ro
可変遅延器
71
61
被測定データ信号
クロック信号
70

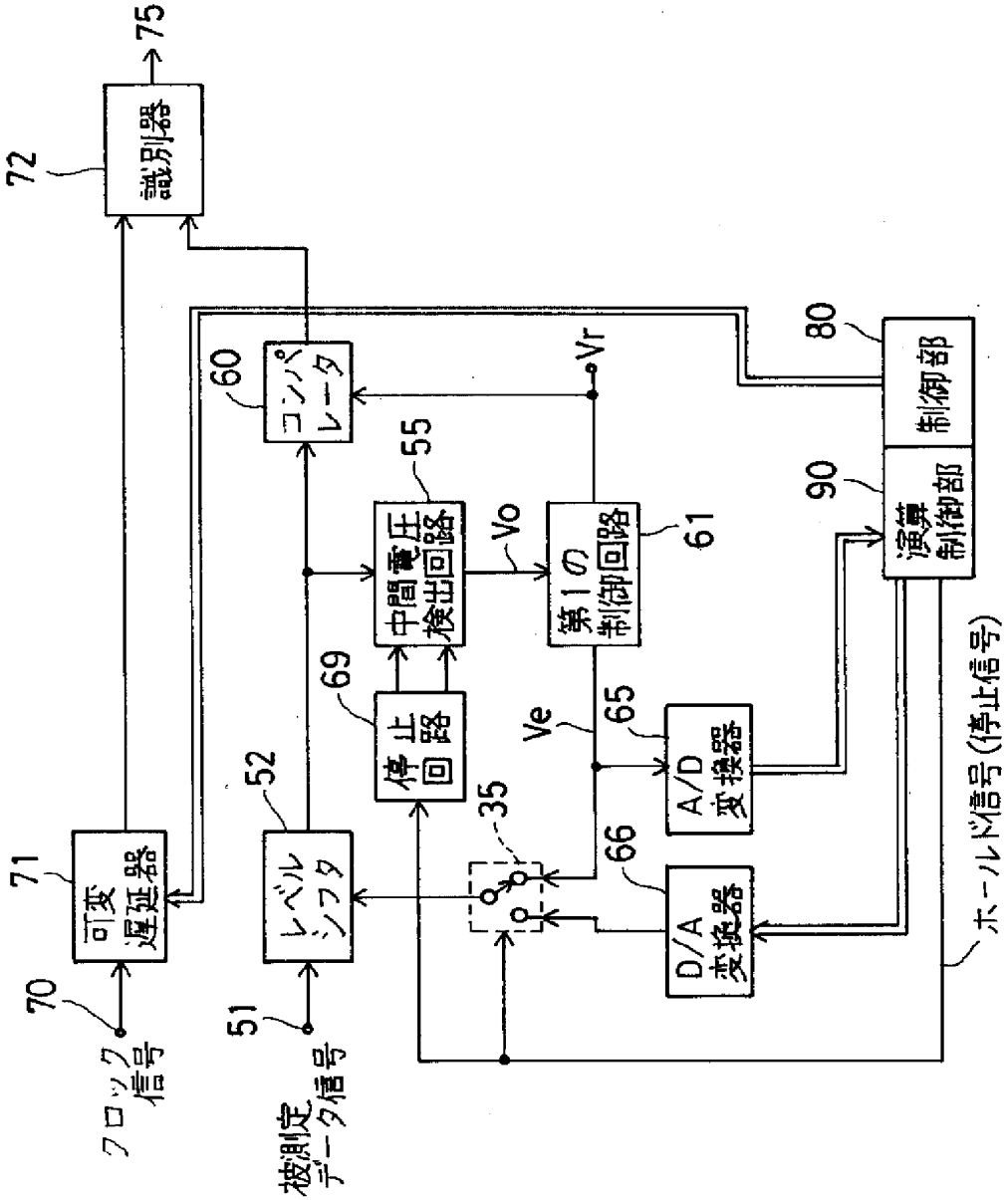
【図１３】


52
60
51
レベルシフタ
コンパレータ
72
Ro
55
56
57
R
R
Vr
59
Vo
参照電圧発生器
62
66
D/A変換器
A/D変換器
65
90
80
演算制御部
制御部

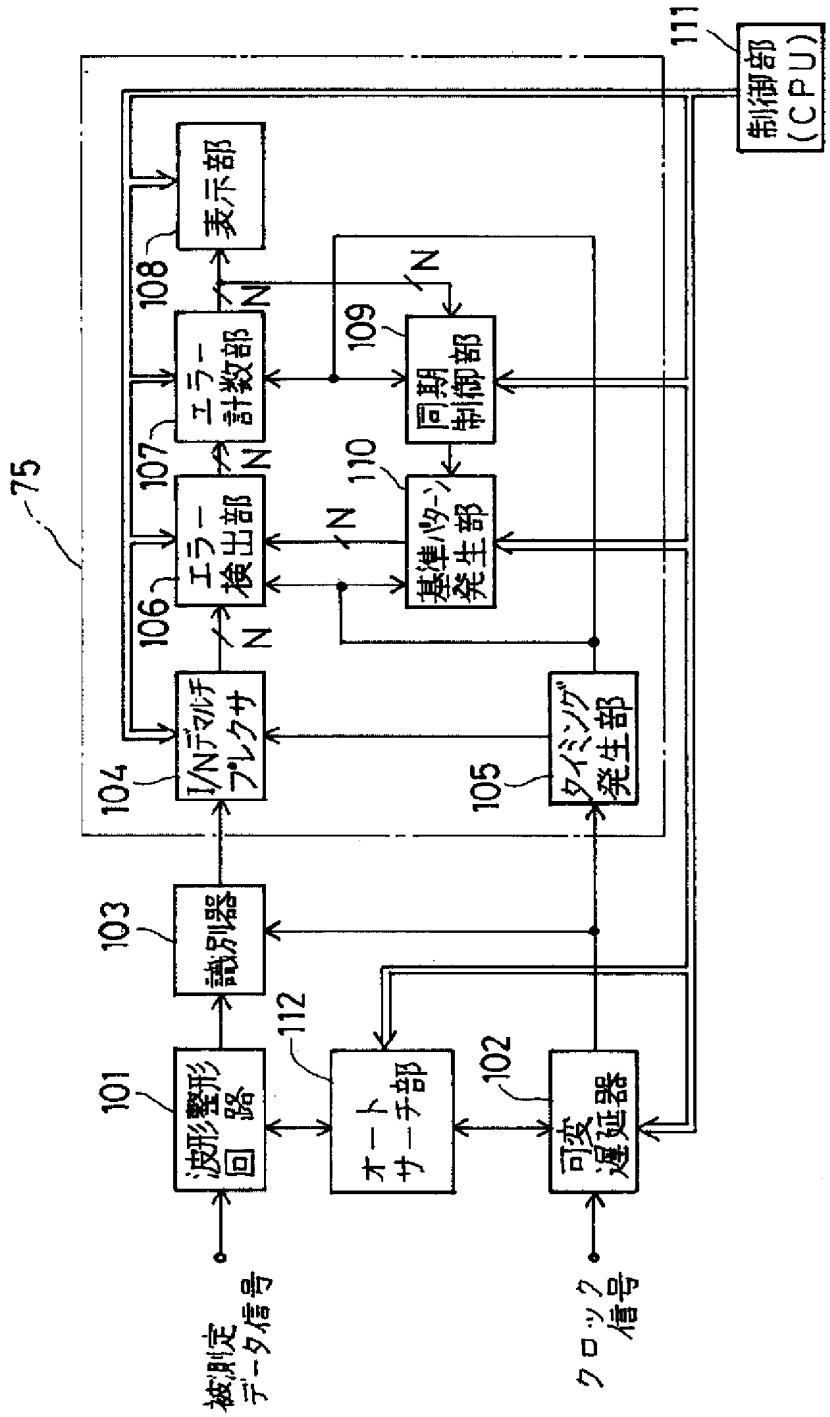
【図１４】


75
72
識別器
80
制御部
60
コンパレータ
Vr
55
中間電圧検出回路
Vo
第１の制御回路
61
52
レベルシフタ
Ve
可変遅延器
71
70
クロック信号
51
被測定データ信号

【図15】


識別器
75
72
コンパレータ
60
Vr
制御部
80
演算制御部
90
中間電圧検出回路
55
Vo
第1の制御回路
61
停止回路
69
Ve
A/D変換器
65
D/A変換器
66
35
可変遅延器
71
レベルシフタ
52
70
クロック信号
51
被測定データ信号
ホールド信号(停止信号)

【図１６】


111
制御部
(CPU)
75
表示部
108
エラー
計数部
107
エラー
検出部
106
1/Nデマルチ
プレクサ
104
109
同期
制御部
110
基準パターン
発生部
105
タイミング
発生部
103
識別器
101
波形整形
回路
112
オート
サーチ部
102
可変
遅延器
被測定
データ信号
クロック
信号
N